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An Investigation on the Short Channel Effect for 0.1μm SOIMOSFET Using Equivalent One Dimensional Model

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Abstract An analytical model for the short channel effect for the SOIMOSFET is proposed. The two dimensional potential problem is reduced to a one dimensional problem, using a virtual electrode which is equivalent to the drain and the source electrodes. The behavior for the short channel effect is also discussed using this model.

1.Introduction

The SOIMOSFET is suitable for device miniaturization, because the shallow junction formation is easy[1]. However, since its property is very sensitive to its structure[2], a clear understanding on the short channel effect is required. For this purpose, this paper proposes an analytical model, using a virtual electrode which is equivalent to the drain and the source electrodes. The electric field from the source and the drain electrodes, which causes the short channel the short channel effect , is replaced by an equivalent electric field from a virtual electrode. The degradation on the subthreshold swing (an increase in the S factor) is analyzed by considering the relation between the gate capacitance and the equivalent capacitance.

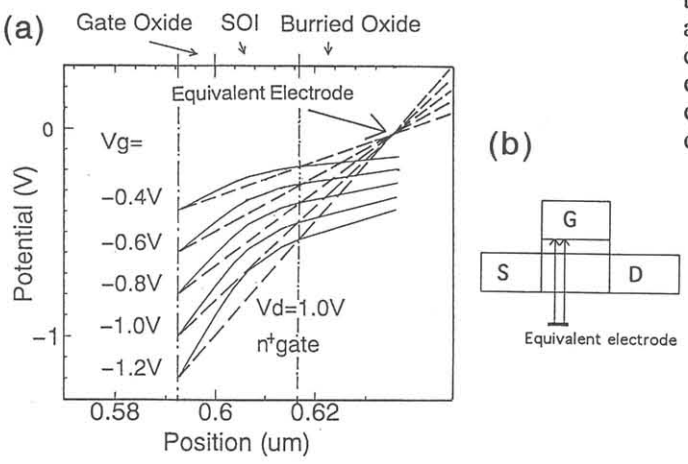

Figure 1 (a) vertical potential profile for 0.2 μm SOIMOSFET at the potential barrier. SOI thickness is 500A, gate oxide thickness is 75A. (b) The electric field from equivalent electrode.

2.Model

The solid lines in Fig. 1a show the potential profile in the vertical cross section for the 0.2μm accumulate mode SOIMOSFET, which is obtained by 2D device simulator. The horizontal position for the cross-section corresponds to the potential barrier. The SOI thickness in Fig. 1 is reduced, in order to correct the discontinuity for the dielectric constant between Si(ε_{Si}) and SiO_2(ε_{OX}), according to the ratio between ε_{OX} and ε_{Si} . With extrapolating the potential gradient between the gate electrode and the SOI back interface, as shown by broken lines, it is found that the lines cross at one point, independently from the gate voltage. This point indicates the position for the virtual electrode, which produces a one dimensional electric field which is equivalent to the two dimensional electric field produced by the drain and the source electrodes (Fig.1b). From a systematical analysis, it is found that the virtual electrode position does not depend on the bias voltage, only the virtual electrode voltage changes. This indicates that the virtual electrode position has a characteristic value for a certain device structure.

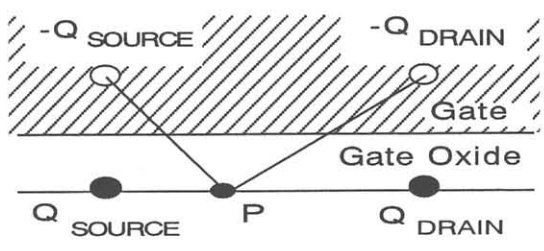

Figure 2 Image charge model to determine the potential barrier position.

The position for the equivalent electrode is derived by combining the analytical solution for the Laplace's equation and the image charge method. Assume an

image charge model, as shown in Fig.2, where the drain electrode and the source electrode are replaced by point charges (Q_{source} and Q_{drain}). The horizontal position of the virtual electrode ,which corresponds to the potential barrier, is given by x which achieves Eq.1.

$$(\phi_d-\phi_g)\{1/x-x/(x^2+4T_{ox}^2)\} = (\phi_s-\phi_g)[1/(L-x)-(L-x)/\{(L-x)^2+4T_{ox}^2\}] \quad (1)$$

Here, ϕ_d is the drain potential, ϕ_s is the source potentia and L in the channel length. The gate potential is assumed to be -0.5V. The potential $\phi(x,y)$ is derived from Laplace's equation by modifying Woo's method[3]. His method combines two boundary conditions, one is for the electric field from the source, and another is for the drain, as shown in Fig.3a. He reported that the dielectric constant discontinuity between ε_{Si} and ε_{OX} can be corrected by an approximation using uniform dielectric constant (ε_{Si}) and enlarging oxide thickness, when the horizontal electric field is small. However, the short channel SOIMOSFET has large horizontal electric field, this correction is not applicable. Therefore, an approximation using a uniform equivalent dielectric constant ε_{equi}, which is given by Eq.2, is introduced.

$$\varepsilon_{equi} = \{\varepsilon_{Si}T_{SOI} + \varepsilon_{OX}(T_{OX}+AT_{BOX})\} / (T_{SOI} + T_{OX}+AT_{BOX}) \quad (2)$$

Here, T_{OX} is the gate oxide thickness, T_{SOI} is the SOI thickness and T_{BOX} is the buried oxide thickness. A is a constant whose value is assumed to be 0.1.when the SOI layer is thin, ε_{equi} approaches ε_{OX}, and when SOI is thick, ε_{equi} approaches ε_{Si}. The equivalent oxide thickness T_{ox}', the equivalent silicon thickness T_{SOI}' and the equivalent buried oxide thickness T_{BOX}', are determined from ε_{equi}, as follows.

$$T_{OX}' = T_{OX}\,\varepsilon_{equi}/\varepsilon_{OX}$$
$$T_{SOI}' = T_{SOI}\,\varepsilon_{qui}/\varepsilon_{Si}$$
$$T_{BOX}' = T_{BOX}\,\varepsilon_{equi}/\varepsilon_{OX} \quad (3)$$

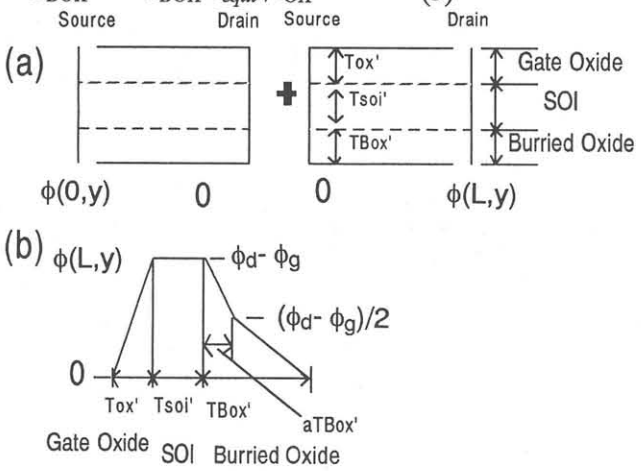

Figure 3 The boundary condition to solve the Laplace's Equation. a is a constant, whose value is assumed to be 0.1

Based on the above assumption, a boundary condition is obtained as in Fig3b. Here, the electric field in the buried oxide is approximated by a bent line. The potential $\phi(x,y)$ is given by Eq.4, using Woo's method.

$$\phi(x,y) = \phi_g + \sum \{a_n(\phi_s-\phi_g)+c_n(\phi_d-\phi_g)\}\sin(n\pi\, y\, L/b)$$

$$a_n = \sinh(n\pi x/b)/\sinh(n\pi L/b)(2/n\pi)(A_n)$$
$$c_n = \sinh(n\pi(L-x)/b)/\sinh(n\pi L/b)(2/n\pi)(A_n)$$
$$A_n = b/n\pi[(\sin(n\pi T_{OX}'/b)/T_{OX}' + 1/(2aT_{BOX}')\sin\{n\pi(T_{OX}'+T_{SOI}')\} + (2a-1)/\{2a(1-a)T_{BOX}'\}\sin\{(n\pi(T_{OX}'+T_{SOI}'+aT_{BOX}')/b)\}$$
$$b = T_{OX}'+T_{SOI}'+T_{BOX}' \quad (4)$$

Since the depth for the equivalent electrode does not depend on the gate voltage, the depth of the equivalent electrode(y_e) which gives the potential for a position y_1, is defined as y which achieves Eq.5.

$$d/d\phi_g\ [\ \phi_g + \{(\phi(x,y_1) - \phi_g)/y_1\}\ y\ ] = 0 \quad (5)$$

From Eqs.4-5, y_e is obtained as Eq.6.

$$y_{equi} = \frac{y_1}{\Sigma\,(a_n+c_n)\sin(n\pi y_1/b)\,(n\pi/b)} \quad (6)$$

The value for y_e is determined uniquely , as long as the potential for SOI layer is linear to the gate voltage. This condition is achieved at the subthreshold regime,where the inversion does not occur. The relation between the S factor and the position of the equivalent electrode is derived by Eq.7.

$$S = (kT/q)\,(\ln 10)\,y_{equi}/(y_{equi}-y_i) \quad (7)$$

Here, y_i is the position where the subthreshold current flows.

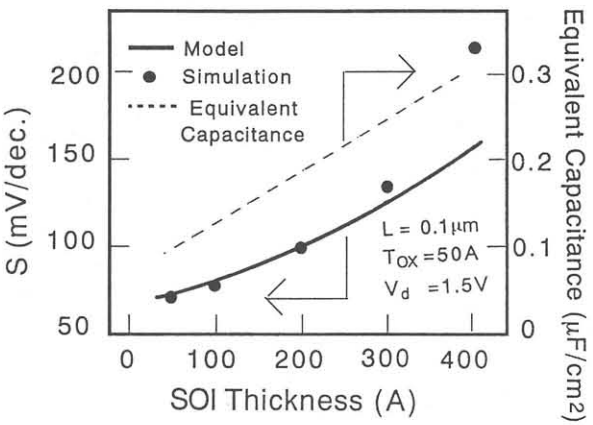

Figure4 S factor dependence on the SOI thickness

3.Result

The solid line in figure 4 shows the S factor dependence on the SOI thickness, for the 0.1um SOIMOSFET,

having 50A gate oxide and 4000A buried oxide, which is obtained by the present model. The result agree with the simulation results, which are represented by solid circles. The broken lines show the equivalent capacitance (the capacitance between the channel and the equivalent electrode). The equivalent capacitance increases with the SOI thickness increasing.powers of SOI thickness. Figure 5 shows *S* factor dependence and the equivalent capacitance dependence on the drain voltage for the 0.1μm SOIMOSFET, having 50A gate oxide, 100A SOI thickness and 4000A buried oxide. This result shows that the S factor and the equivalent capacitance increases with the drain voltage increasing. The reason is that the potential barrier moves toward the source electrode with the drain voltage increasing, e.g. A to B or C in Fig.6, and, consequently, the equivalent capacitance increases, since the capacitance between the source and the channel increases drastically. This effect increases the electric coupling between the channel and the equivalent electrode, and degrades the gate controllability. This indicates that the reduction on the source to the channel capacitance, that is, thin source electrode or LDD structure at source, is efficient to improve the subthreshold characteristic, as well as drain structure. Figure 7 shows potential barrier dependence on the accepter concentration for 0.2μm SOIMOSFET. The broken lines show the potential for the barrier, which is formed at the SOI surface, and the solid lines shows the potential of the barrier which is formed at the SOI back interface. When the barrier is formed at the surface, the S factor is small (the gradients of the lines are steep), since the gate to channel capacitance is large. This led to an excellent gate controllability. In contrast, when the barrier is formed at the back interface, the S factor is large, since the gate to channel capacitance is small, because the distance between the channel and the gate is large. As the accepter concentration increases, the potential distribution changes. This led to an increase in the bias area for surface conduction, where the S factor is improved.

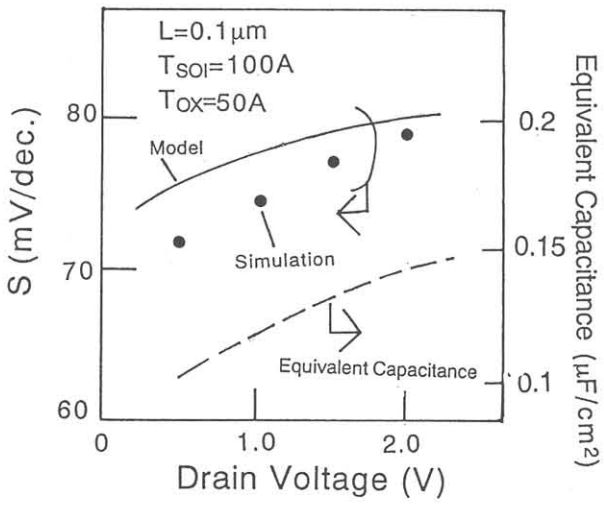

Figure 5 The S factor dependence on the drain voltage.

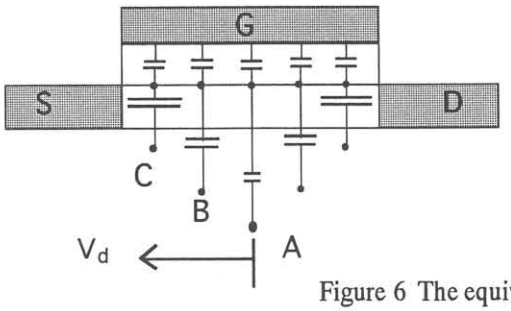

Figure 6 The equivalent capacitance dependence on the drain voltage.

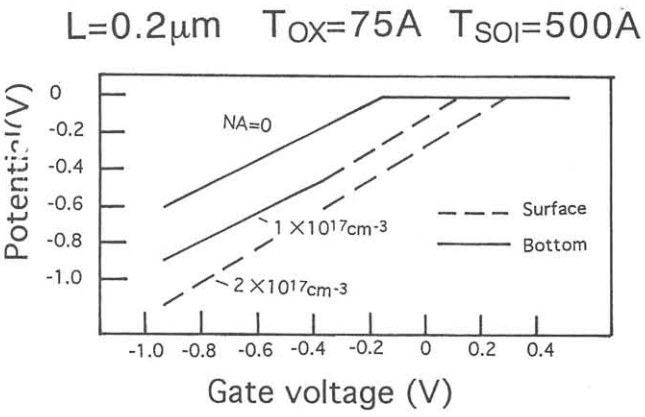

Figure 7 The potential barrier dependence on the gate voltage. Accepter concentration is varied. The potentia is calculated by combining the electric field from equivalent electrode and the acceptors.

4.Conclusion An analytical model for the SOIMOSFET short channel effect is proposed. It is shown that the model is applicable for the estimation and interpretation of the 0.1um SOIMOSFET.

References

[1] Ohmura et.al IEDM Tech.Dig p.675 (1991)
[2] Yoachim et.al 1993 SSDM p.473 (1993)
[3]Woo et.al IEEE ED-37 p.1999 (1990)