Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 298-300

Scaling Merits of Ultra Thin Film SOI/CMOSFET's for Low Power Dissipation

S.Warashina, O.Tsuboi, K.Sukegawa, and N.Sato

Fujitsu Ltd. Process Development Dept.

1015, Kamikodanaka, Nakahara-ku, Kawasaki 211, Japan

We analyzed the power dissipation of ultra thin film SOI/CMOSFETs using a mixed-level device-circuit simulator at 1 V. Difference of the power dissipation between SOI/CMOSFET and bulk/CMOSFET comes from reduction of the drain-substrate capacitance. As device size decreases, the power dissipation ratio of SOI/CMOSFET to bulk/CMOSFET decreases.

1. Introduction

The ultra thin film SOI/CMOSFET, with its reduced drain-substrate capacitance and high conductance, operates well at high frequencies and low power. Also, steep subthreshold characteristic leads to low supply voltages. Using the simulator, we compared the power dissipation of the ultra thin film SOI/CMOSFET operating at 1 V, with the bulk/CMOSFET.

2. Simulation

Our process simulator calculated the 2D-impurity profile of the ultra thin film SOI/CMOSFET. Using this profile, the mixed-level device-circuit simulator[1] ran. Fig. 1 shows the device structure of SOI. Vth of NMOS is 0.2 V, and that of PMOS is -0.2 V by adjusting the doping concentration of channel region. Since the gates of NMOS and PMOS are N-type silicon, PMOS whose channel is P-type is the accumulation mode transistor.

We simulated the 4-stage CMOS buffer. The input sine wave had a 0.5 V amplitude and fin frequency. And the load capacitances of the 3rd and 4th stage were 0.04 pF.

The power dissipation of the ultra thin film SOI/CMOSFET is divided into 5 elements(Fig. 2),

(a) Isc: short circuit current
(b) Igt: gate capacitive energy dissipation of the next stage
(c) Ibd: backgate-drain capacitive energy dissipation of the stage
(d) Icl: load capacitive energy dissipation of the stage
(e) Idg: drain-gate capacitive energy dissipation of the stage

and the total current is Ito.

We calculated Isc, the minimum NMOS and PMOS source current by averaging the shadow area of Fig. 3. We calculated Igt by averaging the positive gate current for the periodic time T(Fig. 4). Ibd and Icl are calculated as well. Ito is the average of the NMOS or PMOS source current. Ito subtract (a)~(d) is Idg.

3. Results and Discussion

The power dissipation dependance of channel length L at 300 MHz is shown in Fig. 5. Igt and Idg are in proportion to L. The power dissipation dependence on gate oxide thickness Tox is shown in Fig. 6. Igt and Idg are in inverse proportion to Tox. Thus shortening L decreases the power dissipation, but thinning Tox increases the power dissipation.

A comparison between SOI/CMOSFET and bulk/CMOSFET at 100 MHz is shown in Fig. 7. Ibd of SOI/CMOSFET is smaller than that of bulk/CMOSFET, because of reduction of drain-substrate capacitance. The Ito of SOI/CMOSFET is 15% smaller than that of bulk/CMOSFET.

We will think about a power dissipation advantage of SOI/CMOSFET to bulk/CMOSFET when we deduct device size. Then both L and Tox decrease. Igt and Idg are constant, as they are in proportion to L/Tox. Ibd is in proportion to N/ld. N, which is shown in Fig. 1, is the length of source and drain. ld of SOI/CMOSFET is the thickness of the backgate oxide, and ld of bulk/CMOSFET is the width of the depletion area. Ibd is the length between drain and substrate. Therefore Ibd of SOI/CMOSFET is constant. But Ibd of bulk/CMOSFET increases as the impurity concentration of substrate increases to decrease the short channel effect. As a result, the power dissipation of bulk/CMOSFET increases. On the other hand, that of SOI/CMOSFET is constant. Hence, if we reduct device size, the power dissipation ratio of SOI/CMOSFET to bulk/CMOSFET decreases.

4. Conclusion

We analysed the power dissipation of the buffer circuit consisting of the ultra thin film SOI/CMOSFET at 1 V operation using the mixed-level device-circuit simulator.

○Difference of the power dissipation between SOI/CMOSFET and bulk/CMOSFET comes from reduction of the drain-substrate capacitance. The power dissipation of SOI/CMOSFET is 15% smaller than that of bulk/CMOSFET.

○If we reduct device size, the power dissipation ratio of SOI/CMOSFET to bulk/CMOSFET decreases.

Reference

1) S.Satoh et al,"Parallel Computing Using a Mixed-Level Device-Circuit Simulator," VPAD (1993)p.128.

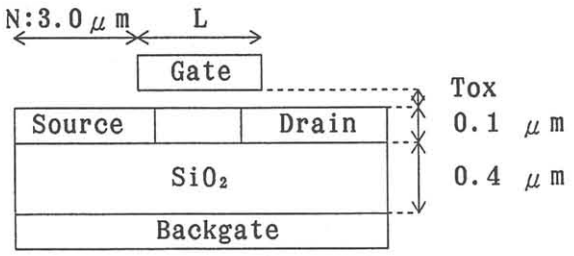

Fig.1 Device structure of SOI

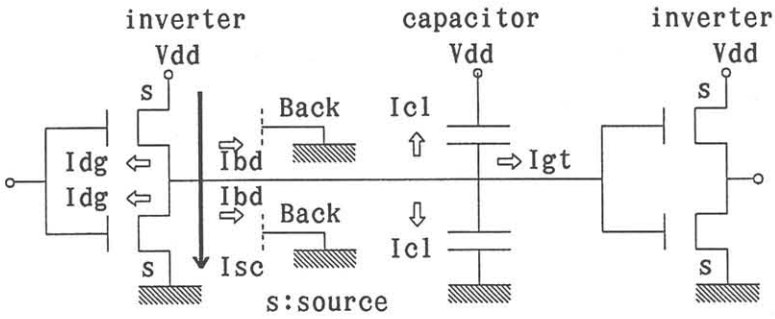

Fig. 2 Analysis of power dissipation

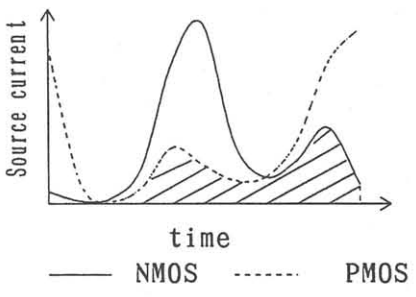

Fig. 3 Calculation of Isc

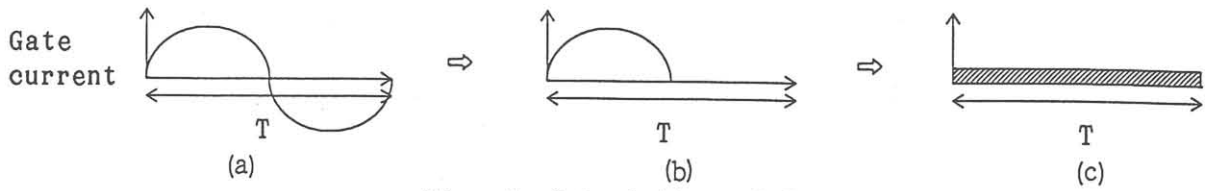

Fig. 4 Calculation of Igt

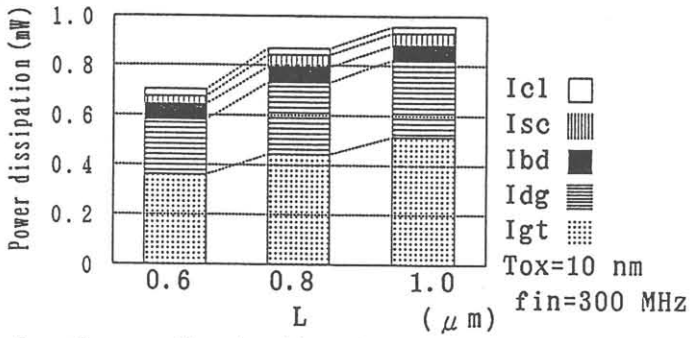

Fig. 5 Power dissipation dependence on L of SOI

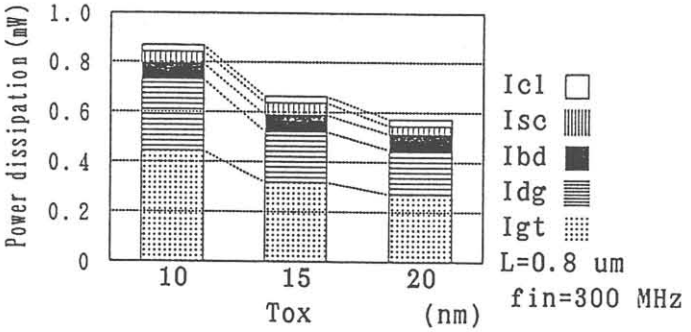

Fig. 6 Power dissipation dependence on Tox of SOI

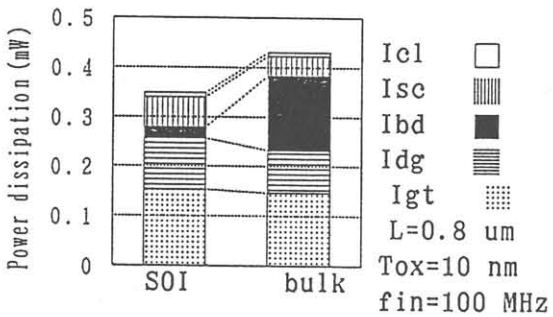

Fig. 7 Comparison between SOI and bulk