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# Two-Dimensional Analytical Modeling of the LDD Condition Influence on Short-Channel Effects in SOI MOSFET's

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The scaling of MOS devices into the deep-submicron regime brings about an increasing influence of source/drain engineering on the transistor subthreshold characteristics.This paper presents a theoretical analysis of how source/drain conditions affect the short-channel behavior of fully depleted SOI MOSFET's. Two-dimensional analytical modeling gives insight into the mechanisms involved. The results, supported by numerical device simulation, indicate that for an accurate description in addition to the different source and drain junction built-in potential an increasing effective gate length with LDD doping reduction has to be taken into account.

## INTRODUCTION

The ongoing scale-down of MOS transistor device dimensions has already led into gate length regions of less than a tenth of a micron. Silicon-on-Insulator (SOI) MOSFET's are considered a promising candidate for deep-submicron applications due to their improved device and circuit performance[1]. In order to alleviate floating body effects and source-to-drain breakdown voltage lowering, a lightly doped source and drain region (LDD) is often utilized. Usually, a trade-off is necessary because of device transconductance reduction by the LDD resistance. For very short gate length, however, the LDD conditions may also influence the subthreshold device characteristics.

Although numerical device simulation is widely used to predict and investigate the performance of deep-submicron structures, analytical models are desired owing to their ability to easily demonstrate parameter dependencies and to reveal the mechanisms behind certain effects observed. Such models should be as easy as possible while being as accurate as necessary. For the analysis of short-channel effects a completely two-dimensional description is mandatory.

In this paper, such an analytical model for the fully depleted SOI MOSFET is presented and applied to the investigation of the LDD condition influence on the short-channel subthreshold device characteristics. The results are supported by numerical device simulation.

## ANALYTICAL MODEL

The schematic cross section of an n-channel SOI MOSFET is depicted in Fig.1. In order to model the

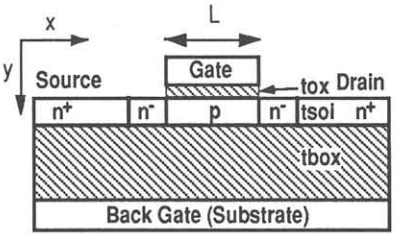


**Fig. 1 Schematic cross section of the n-channel SOI MOSFET structure (L=0.15μm, tox=60Å, tsoi=250Å, tbox=3800Å)**

potential distribution inside the p-type channel, the two-dimensional Poisson's equation is solved by assuming a parabolic channel potential distribution in y-direction. This approach has been proposed by Young[2] who, however, used an inappropriate linear potential boundary condition at the SOI/buried oxide interface. The simulated vertical potential through the SOI structure shown in Fig. 2 clearly gives a nonlinear potential variation inside the buried oxide. This is due to source and drain electric fields which influence the

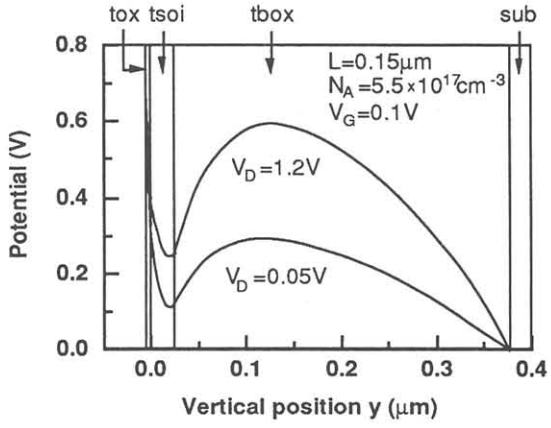


**Fig. 2 Simulated vertical potential through the SOI-structure at x=L/2 showing the nonlinearity inside the buried oxide**

channel potential through the buried oxide in short-channel transistors even at low drain voltage $V_D$. Consequently, Young's model underestimates the drain-induced-barrier-lowering (DIBL) effect. To account for the accurate boundary condition while keeping the relative simplicity of the model, we introduce an effective substrate voltage $V_{SUB}^{eff}$. This voltage is chosen to obtain the same electric field at the SOI/buried oxide interface as with the real nonlinear potential. The $V_{SUB}^{eff}$-concept has already been successfully applied to subthreshold slope factor modeling by extracting the voltage from numerical simulation results[3]. However, a suitable calculation method for $V_{SUB}^{eff}$ is desired. By rigorously solving the Laplace's equation inside the buried oxide, the following expression can be derived

$$V_{SUB}^{eff} = \sum_{m=1}^{\infty} \sin\left(\frac{m\pi}{L}x\right)\left[c_{fm}V_G + c_{bm}V_{SUB} + c_{sm}\right] \quad (1)$$

where $V_G$ and $V_{SUB}$ are the gate voltage and the real substrate voltage applied to the device including the corresponding flatband voltages, and $c_{fm}$, $c_{bm}$ and $c_{sm}$ are obtained as Fourier coefficients. Although the sum in eq. (1) converges quickly, a further simplification can be made for the determination of $V_{SUB}^{eff}$. Since $c_{fm}$ and $c_{bm}$ only depend on structural parameters and $c_{sm}$ is a linear function of the channel doping level $N_A$, the built-in potential $\Phi_{bi}$ and the drain voltage $V_D$, for a given structure and a variation of these parameters a simple linear relationship can be obtained from calculating the sum of eq. (1) only once with the desired derivative .

From the solution of the Poisson's equation the minimum potential at the front gate oxide/silicon interface can be derived which leaves a parabolic equation for the threshold voltage to be solved. The final expression for the threshold voltage in this model is obtained as

$$V_{th} = V_{FB}^{f} + \left(\frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}\right)^{-1}\left[\left(1 + 2\frac{C_{SOI}}{C_{BOX}}\right)\frac{qN_A t_{SOI}^2}{2\varepsilon_{Si}} - \left(V_{SUB}^{eff} - V_{FB}^{b}\right)\right.$$

$$\left. - \left(1 + \frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}\right)\frac{\psi_{th} - 2SH\left(2SH\left(\Phi_{bi} + V_D/2\right) + \sqrt{\left(\Phi_{bi} - \psi_{th}\right)\left(\Phi_{bi} + V_D - \psi_{th}\right)}\right)}{1 - 4SH^2}\right] . \quad (2)$$

Thereby, $C_{OX}$, $C_{SOI}$ and $C_{BOX}$ are the capacitances of the gate oxide, SOI layer and buried oxide, respectively, $V_{FB}^{f}$ and $V_{FB}^{b}$ are the flatband voltages of the front and back gates, and $\psi_{th}$ is the threshold potential (usually twice the Fermi-level for inversion mode transistors). SH is given by the following expression

$$SH = \frac{\sinh\left(L^*/2\right)}{\sinh\left(L^*\right)} \quad (3)$$

with

$$L^* = L\sqrt{\frac{2\left(1 + \frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}\right)}{t_{SOI}^2\left(1 + 2\frac{C_{SOI}}{C_{BOX}}\right)}} \quad . \quad (4)$$

The term SH describes the short-channel effects which arise from the boundary conditions at the source and drain ends of the channel. With increasing gate length SH approaches zero while $V_{SUB}^{eff}$ tends to the real $V_{SUB}$. Therefore, eq. (2) naturally reduces to the result of one-dimensional modeling for long-channel devices.

## MODEL APPLICATION AND DISCUSSION

Fig. 3 shows the threshold voltage dependence on LDD doping concentration for a 0.15µm gate length transistor with ultra thin-film SOI of $t_{soi}$=250Å at two different drain voltages. The solid lines are obtained from eq. (2) by simply adjusting the built-in potential $\Phi_{bi}$ according to the $n^-$-concentration. A linear $V_{th}$-increase is predicted when reducing the doping of LDD from the single drain level.

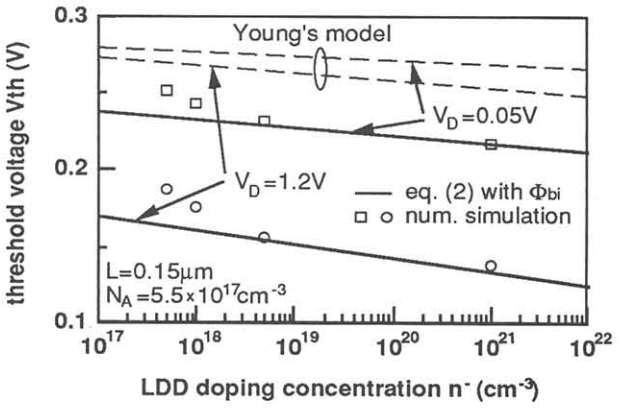


**Fig. 3 Threshold voltage vs. LDD concentration**

The symbols in Fig. 3 represent numerical simulation results for comparison. It must be noted, that the single drain threshold voltage ($n^-$=10$^{21}$cm$^{-3}$) and the correct slope are only reproduced correctly if the effective substrate voltage according to eq. (1) is incorporated. It has an additional linear dependence on $\Phi_{bi}$ which itself is proportional to the log of the $n^-$-concentration. Without $V_{SUB}^{eff}$ the model would predict a more long-channel-like behavior due to the ultra-thin SOI layer (SH small) with a by far too weak drain voltage influence. This is illustrated by the dashed lines in Fig. 3. The importance of the correct boundary condition confirms the fact that for thin-film SOI MOSFET's the main part of the source/drain region influence happens by way of the buried oxide.

From the symbols of numerical device simulation results in Fig. 3 it is obvious that for lower LDD concentration a stronger than linear increase of $V_{th}$ occurs. Therefore, an additional mechanism has to be considered. This is schematically illustrated in Fig. 4 where the potential

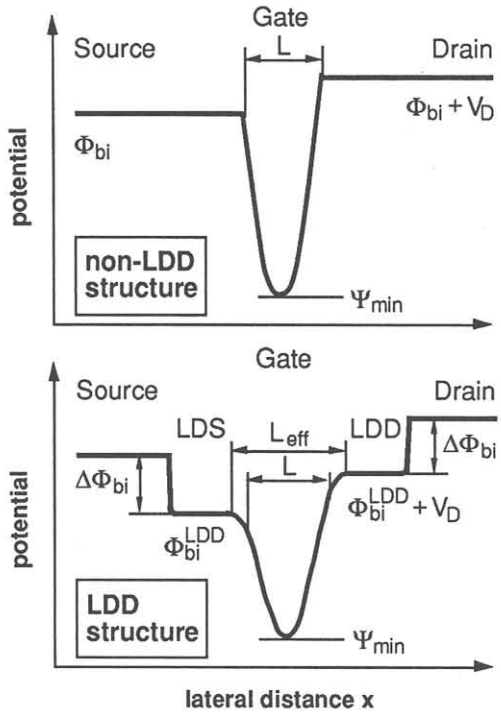


**Fig. 4 Schematic illustration of the lateral potential profile for non-LDD and LDD structure showing the built-in potential shift $\Delta\Phi_{bi}$ and the change in $L_{eff}$**

profile from source to drain for the non-LDD and LDD transistor structure is drawn. Due to a comparable level of the channel and the LDD doping concentration the penetration of the depletion layer into the LDD region cannot be neglected leading to an increase of the effective gate length and therefore to a reduction of the short-channel $V_{th}$ roll-off, i.e. to a higher threshold voltage. The amount of change in the effective gate length can be estimated with sufficient accuracy by calculating the corresponding depletion width inside the LDD region from simple pn-junction theory. This is demonstrated in Fig. 5 where the calculated results are compared with the gate lengths obtained by numerical

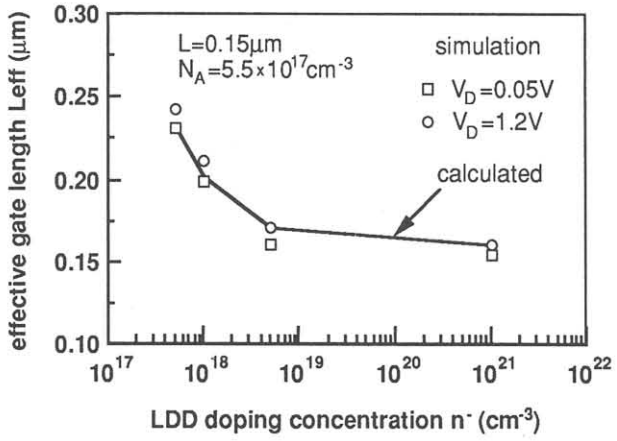


**Fig. 5 Comparison of the effective gate length vs. LDD concentration calculated from simple pn-junction theory and extracted from numerical simulation results**

simulation. There is virtually no dependence on the drain voltage and a good agreement is observed.
Taking this effect into account the threshold voltage for the LDD transistor is obtained by first calculating the built-in potential $\Phi_{bi}$ and the effective gate length $L_{eff}$ for the corresponding LDD doping concentration and then using these values in eqs. (1-4) substituting $L_{eff}$ for L. By doing so the solid curves in Fig. 6 are obtained which fit well with the simulation results and verify the assumed mechanism of the LDD influence.

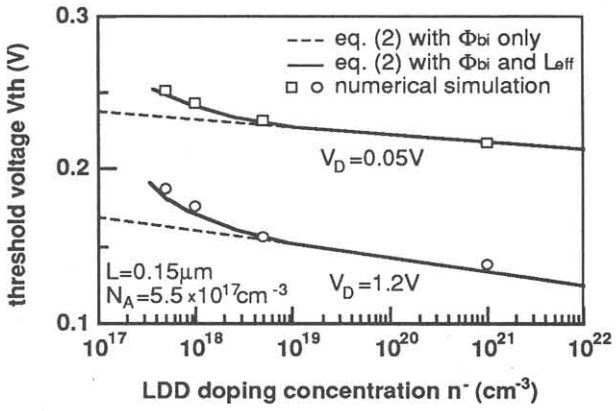


**Fig. 6 Threshold voltage vs. LDD concentration comparison between the analytical model and numerical device simulation results**

Generally, if one considers the difference between the threshold voltages of the single drain (non-LDD) and a certain LDD structure as a measure for this influence, it is found that the sensitivity of $V_{th}$ to the LDD conditions vanishes exponentially with increasing gate length. The critical L, below that the influence is observed, is smaller for thinner SOI film.

## CONCLUSION

The influence of the LDD conditions on subthreshold transistor characteristics has been investigated for deep-submicron fully depleted SOI MOSFET's. A two-dimensional analytical model which takes into account the correct SOI/buried oxide boundary condition by means of an effective substrate voltage has been developed and provides insight into the mechanisms involved. It has been found that both the reduction of the built-in potential and an increase of the effective gate length have to be considered when modeling devices with lower doped LDD regions. Good agreement with numerical simulation results suggest that the model can be utilized to predict design criteria for high performance 0.15µm gate length SOI MOSFET's.

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[2] K. K. Young, IEEE Trans. Electron Devices 36 (1989) 399
[3] H.-O. Joachim et. al., IEEE Trans. Electron Devices 40 (1993) 1812