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Intelligent Power IC with Partial SOI Structure

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In the integration of power devices and control circuits, temperature rise caused by the heat dissipation of power devices and electric interference between power devices and control circuits are important problems. By using the partial SOI structure with shield layer, we demonstrated that the temperature rise was reduced to about a half of that in the complete SOI structure and the latch-up occurrence in control circuit was prevented. And at the condition of 150 ℃ and 16V, the normal operation of intelligent power IC consisting of power devices and 1 bit micro-computer was accomplished.

1.Introduction

Several types of intelligent power IC have been developed for use of automotive electronics, flat panel display and motor power supply. [1)2)3)] In the use of automotive electronics, it is necessary to reduce the temperature rise caused by the heat dissipation of power devices because the intelligent power IC is used in high temperature environmental condition. The protection from electric surge in automotive environment and the immunity of the electric interference between power devices and control circuits are also required. Furthermore, taking the trend of the automotive electronics into consideration, the function for communication and multiple outputs are required.

For the integration of power devices and control circuits on a single chip, the self isolation ,the pn-junction isolation and the dielectric isolation are used as the separation structure. [4)] From the point of view of flexibility of IC design, high packing density and reliability, the die electric isolation is superior to others. In the dielectric isolation , especially we have used partial Silicon-On-Insulator (SOI) structure for the purpose of the integration of Vertical-Double-Diffused MOS (VDMOS) power devices and control circuits as shown in Fig.1.[5)]

In this report, firstly, the temperature rise and the electric interference in the partial SOI structure that we have already proposed are described. Secondly ,the trial result of an intelligent power IC consisting of multi-channel power devices and a built-in 1 bit micro-computer is described.

2. Device Structure and Fabrication

The cross-sectional view of the intelligent power IC with partial SOI structure is shown in Fig.1. The most significant feature of the partial SOI structure is it has SOI area and Si directly bonded area. As shown in Fig.1 some control circuits are formed in the SOI area and the VDMOS power devices are formed in the Si directly bonded area. And any devices are isolated each other laterally by trenches. In the conventional complete SOI structure, both of the control circuits and

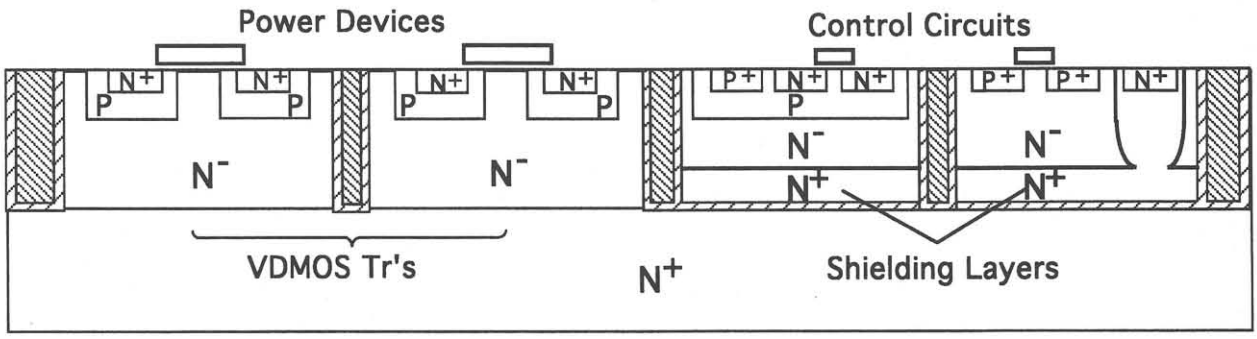
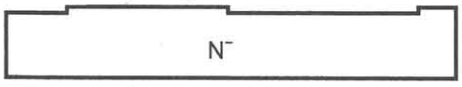


Fig. 1 Cross-sectional view of the intelligent power IC with partial SOI structure

the power devices are formed in the SOI area. Therefore, it is not possible to form VDMOS power devices but alternatively it is possible to form up-drain DMOS in the complete SOI structure.

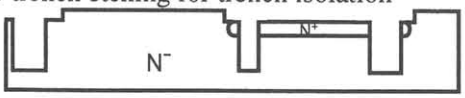
The partial SOI structure was fabricated by wafer direct bonding process as follows,

(1) shallow trench etching for SOI area

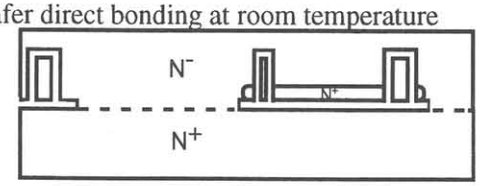


(2) shielding layer formation by As+ ion implantation

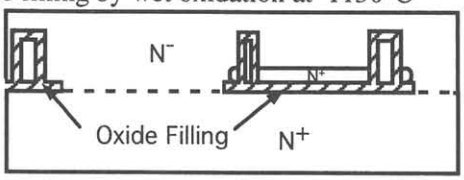
(3) deep trench etching for trench isolation



(4) wafer direct bonding at room temperature



(5) oxide filling by wet oxidation at 1150 ℃



(6) surface grinding and chemical mechanical polishing

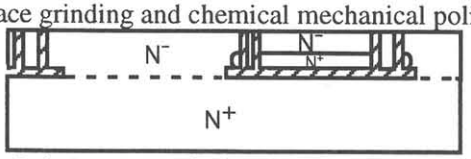


Fig.2 Fabrication of the partial SOI structure

3. Evaluations and Results

3.1 Temperature rise

The heat conductivity of SiO2 is only about 1/100 of that of Si. In complete SOI structure, the heat from power device accumulates in SOI region. On the contrary, in the partial SOI structure, the heat flows easily to the N+ substrate. [6] Therefore, it is expected that the temperature rise can be reduced in the partial SOI structure. Hence, temperature rise was evaluated by measuring the change of I-V characteristics of a pn-diode while the power device was operating. The pn-diodes were formed in power device region and control circuit region. Figure 3 shows the temperature rise of power device region and control circuit region. In comparison with the complete SOI structure, it was clarified that the temperature rise of the power device region and control circuit region were reduced to 55% and 50%,respectively. This result indicates that the power area of the integrated single chip can be reduced to half.

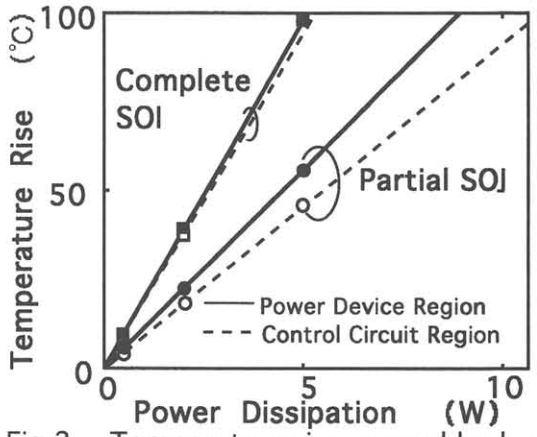


Fig.3 Temperature rise caused by heat dissipation of power devices

3.2 Electric interference

In the Fig.1, the control circuits are separated from the substrate by the oxide film. The substrate voltage fluctuation caused by VDMOS switching operation and supplying voltage fluctuation is transmitted to control circuits and latch-up phenomenon occurs in the control circuits. [5] For preventing the latch-up, the shielding layer is inserted in the bottom of SOI region. To evaluate this effect, the degree of latch-up occurrence was measured as the function of the sharpness of the substrate voltage fluctuation. The structures of no shielding layer, 50 Ω/□ shielding layer and 10 Ω/□ shielding layer were evaluated. Figure 3 shows the results. It was clarified that in the case of 10 Ω/□ shielding layer latch-up does not occur at even 250V/ μ sec. In the use of automotive electronics, the sharpest voltage fluctuation is about 70V/ μ sec. Therefore, this shielding layer is enough effective to prevent the faulty operation.

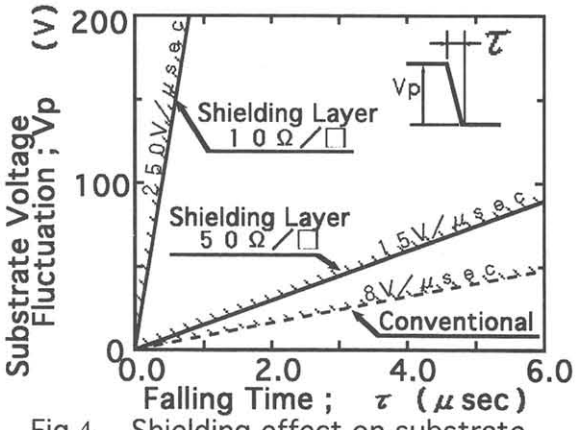


Fig.4 Shielding effect on substrate voltage fluctuation

3.3 System operation

Taking the temperature rise and the electric interference into account, the intelligent power IC with 1 bit micro-computer was fabricated for trial. Figure 5 shows the photograph of the intelligent power IC. 1.5A-class two channel VDMOS devices and two channel up-drain DMOS devices were integrated in the power area.

Overheat detection and protection, overvoltage detection and protection, gate drive circuit and 1 bit micro-computer with mask ROM were integrated in the control circuit. The chip size was 5 mm × 5 mm. The cross-sectional view in Fig.1 corresponds to the cross-section of A-A in the Fig.5.

Table 1 shows the relation between input levels and output levels in the 1 bit micro-computer control. The system operation of the intelligent power IC was evaluated by measuring the output voltage when the input voltage was supplied. As the input voltage, pulse voltage or step voltage was supplied for practical use. Figure 6 shows the result. It was verified that the two channel outputs voltage were controlled without mutual electric interference and they followed the relation in Table 1. And at the condition of 150℃ and 16V, the normal operation of intelligent power IC consisting of power devices and 1 bit micro-computer was accomplished.

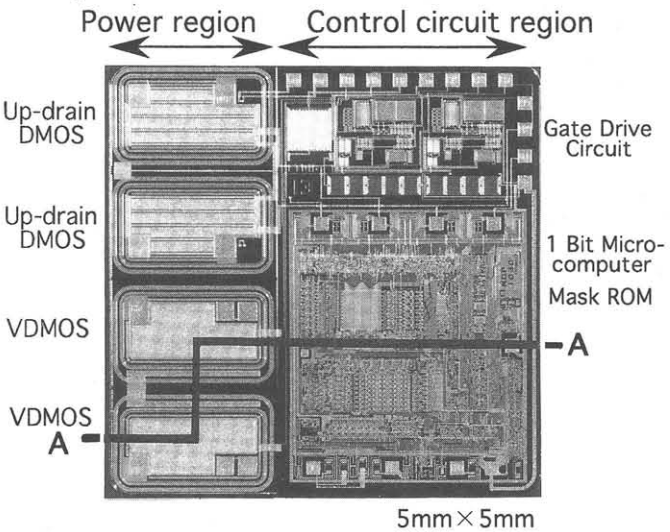


Fig.5 Chip photograph of the intelligent power IC manufactured for trial

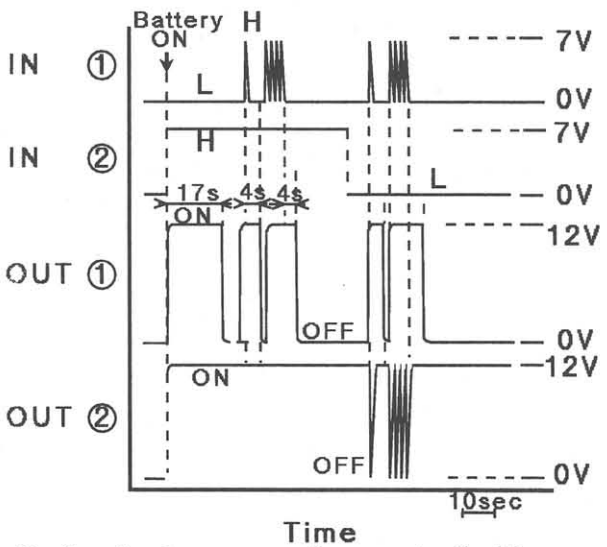


Fig.6 System operation controlled by the software of built-in microcomputer

Table 1

IN ①	L	H	L	H
IN ②	L	L	H	H
OUT ①※1	OFF※2	ON	OFF※2	ON
OUT ②	ON	OFF	ON	ON

※1; Batterry ON
⇒ OUT ① changes to ON for 17sec⇒OFF
※2; IN ①:L
⇒ OUT ① keeps ON for 4sec⇒OFF

4. Conclusion

On the intelligent power IC with partial SOI structure, and the followings were verified.

(1) The temperature rise in the partial SOI structure was reduced to about a half that in the complete SOI structure at the same power dissipation. This result indicates the power area of the integrated single chip can be reduced to half.

(2) On the electric interference in automotive use, it was clarified that the latch-up occurrence in control circuit was prevented by the insertion of 10 Ω/□ shielding layers in the SOI region.

(3) The system operation of the intelligent power IC consisting of multi-channel power devices and a built-in 1 bit micro-computer was demonstrated. It was revealed that at the condition of 150℃ and 16V, the normal operation of the intelligent power IC was accomplished.

Acknowledgements

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