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Dynamic Characteristics of Inverter Circuits Using Single Electron Transistors

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We have investigated basic characteristics of capacitively and resistively coupled SET inverters as a digital logic circuit. Input-output transfer characteristics and dynamic characteristics have been calculated based on the semi-classical model by the Monte Carlo method. Although a voltage gain larger than unity is found even in a cascade connection, they reveal some disadvantages such as small voltage gain, poor input-output separation, small logic level difference, instability of operating point and oscillational output voltages. The switching delay time is estimated to be of the order of 100RC, where R and C is a resistance and a capacitance of a tunnlel junction respectively.

1.Introduction

Recently, single electron digital circuits are attracting many researchers attentions because of their potential performance with very low power consumption and high switching speed. Basic operating mechanism of these circuits are based on the single electron tunneling (SET) effect[1] in very small tunnel junctions. There have been proposed many types of SET devices, such as a capacitively coupled transistor[1], a resistively coupled transistor[1], a complementary logic circuit[2], a turnstile device[3], and a pump device[4], *etc.*, and their basic characteristics have been verified experimentally. In this report, we represent numerical calculations concerning basic characteristics of the capacitively coupled (C-) and the resistively coupled (R-) SET inverters which are loaded by resistance, and examined their transfer characteristics and dynamic properties as a digital logic circuit.

2.Basic Cell and Simulation Method

Figure 1 shows basic cells of C-SET and R-SET inverters. The C-SET inverter (Fig. 1(a)) consists of a C-SET transistor (which is composed of two small tunnel junctions with capacitance C_1, C_2 and resistance R_1, R_2, and an input capacitance C_{in}), a load resistance R_L, and a output capacitance C_{out}, where C_{out} includes a parasitic capacitance of the electrode B and an input capacitance of a next stage inverter. The basic cell is driven by a voltage source V_L. The R-SET inverter (Fig. 1(b)) is a revised version of the C-SET inverter, where C_{in} and C_{out} are replaced by a input resistance R_{in} and an output resistance R_{out}, respectively. In this case, a output capacitance C_{out} is added parallel to R_{out} as a parasitic capacitance of a electrode B.

All calculations in this study are based on the semi-classical model[1], where electron tunneling events in individual tunnel junctions are stochastic process and determined by free energy difference between before and after the tunneling event. Using a junction voltage V and a temperature T, an electron tunneling rate per unit time is given by the following equation

$$\Gamma(V)=\frac{1}{e^2R_t}\frac{\mp eV-E_c}{1-\exp[(\pm eV+E_c)/kT]}, \qquad (1)$$

where R_t is a resistance of the tunnel junction and $E_c=e^2/2C\Sigma$ is a charging energy required in the single electron tunneling. $C\Sigma$ is a total capacitance including the junction capacitance and a parasitic capacitance of the external circuits connected in parallel with the junction. Considering that a total charge in the isolated electrode changes only by an elementary charge e in each tunneling event, we can calculate the time evolution of the electrode charge and hence the junction voltage by determining whether an electron tunnels or not during a

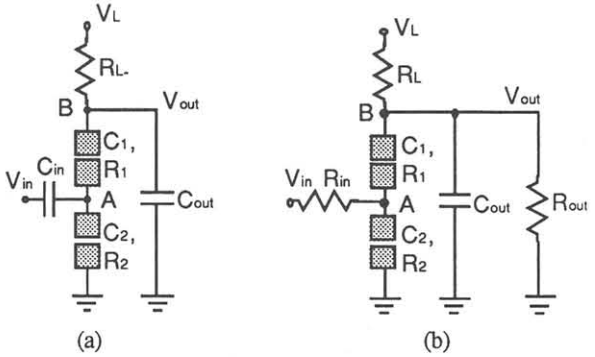

Fig. 1 The inverter circuits using (a) capacitively and (b) resistively coupled SET transistors.

short time period according to the electron tunneling rate eq.(1)[5]. In calculations, we ignore the co-tunneling process and the quantum fluctuation which have to be considered when the resistance of the tunnel junction is not so large comparing with the critical resistance R_C.

3.Static Characteristics of the SET Inverters

Figure 2 shows voltage transfer characteristics of the C-SET and the R-SET inverters for various values of the bias voltage V_L at very low temperature $kT/(e^2/2C_1)$ =0.001 where the thermal fluctuation can be neglected. As can be seen in the figure, the both inverters have voltage gain larger than unity at $V_{in}/(e/2C_1)\approx 0.16$ for the C-SET inverter and at $V_{in}/(e/2C_1)\approx 0.55$ for the R-SET inverter. Although the R-SET inverter has larger voltage gain than the C-SET inverter, an output voltage difference ΔV_{out} which is a difference between logic level "1" and "0" is very small in the R-SET inverter.

By the calculation of the V_L dependence of the maximum voltage gain G_{max} and ΔV_{out}, we find that G_{max} and ΔV_{out} are optimized when $V_L=0.8\sim0.9V_{Lt}$, where V_{Lt} is the bias voltage of the inverters which gives the threshold whether the SET transistor is in a conduction state or in a Coulomb blockade state. Throughout the following calculations, we use the condition $V_L=0.9V_{Lt}$.

Figure 3 shows the dependence of G_{max} of the C-SET inverter on the input capacitance C_{in} and the output capacitance C_{out}. One can see that G_{max} increases with decreasing C_{out} and increasing C_{in}, in the range 2~6. An elementary estimation about the voltage gain gives $G_{max}=-C_{in}/C_1$, which is slightly larger than the simulation results. The discrepancy is arising from the non ideal current biasing. Small G_{max} value at $C_{out}/C_1=2$ and $C_{in}/C_1=20$ is due to the thermal fluctuation which is not negligible when C_{in} is large.

In Fig. 4(a) is shown the dependence of G_{max} of the R-SET inverter on the output resistance R_{out}. It is seen from the figure that the gain of the inverter goes down with decreasing R_{out} (or increasing output load). The reduction of the gain will be serious problems in designing the logic circuits using this injection type device, because it restricts fan-out number. Figure 4(b) shows the dependence of G_{max} on the input resistance R_{in}. There is a maximum G_{max} in the G_{max}-R_{in} relation. The decrease in G_{max} for larger R_{in} is due to the reduction of the rate of charge injection through R_{in} to the center electrode (electrode A in Fig. 1(b)) which triggers and breaks the Coulomb blockade state of the lower tunnel junction. On the other hand, too small R_{in} extracts excess charges on the electrode A, resulting in suppression of the space-correlated tunneling between the two tunnel junctions.

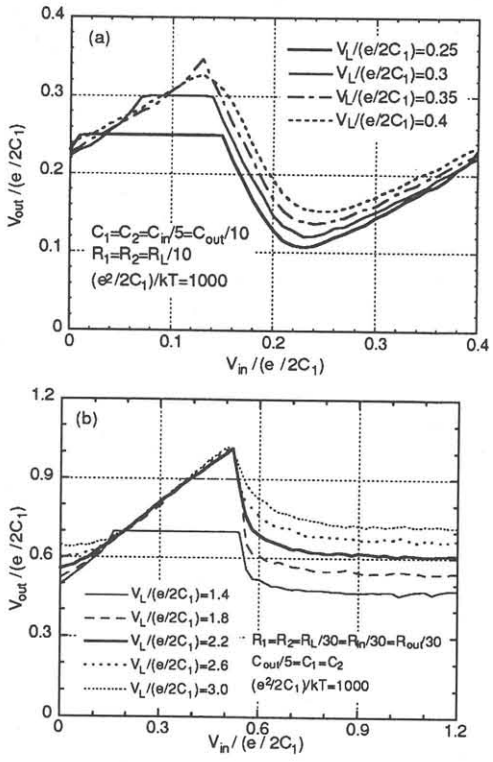

Fig. 2 The voltage transfer characteristics of (a) the C-SET inverter and (b) the R-SET inverter for various values of the bias voltage V_L.

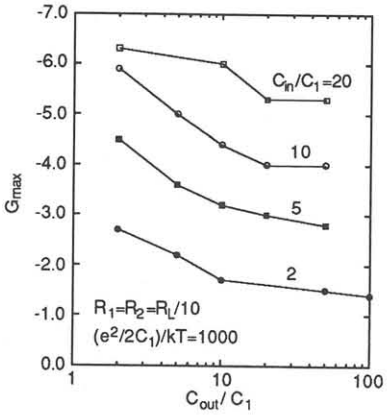

Fig. 3 The dependence of the maximum voltage gain G_{max} of the C-SET inverter on the input capacitance C_{in} and on the output capacitance C_{out}.

We also calculated the dependence of the operation point with the maximum voltage gain on parameters of external circuit elements. The results show that the operating point varies considerably depending on C_{in} and C_{out} in the case of C-SET inverter, whereas the R-SET inverter exhibits only slight change.

4.Dynamic Characteristics of the SET Inverters

Figure 5 shows switching waveforms of the input and output node voltages of the C-SET and the R-SET inverters. It can be seen in the figure that the output waveforms are oscillating function of time connected

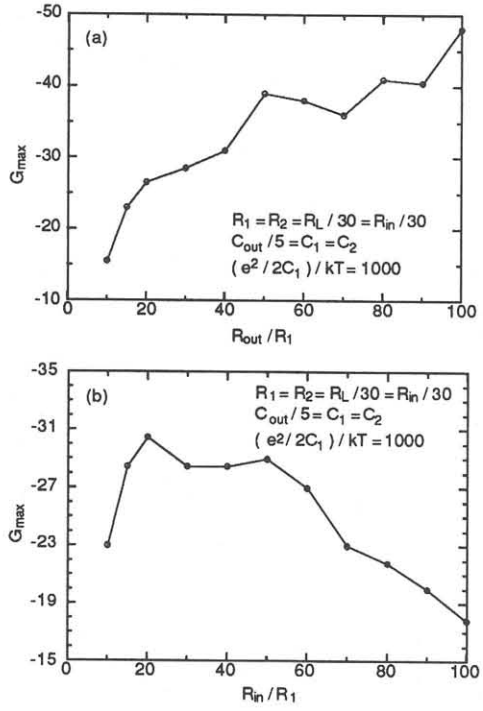

Fig. 4 The dependence of the maximum voltage gain G_{max} of the R-SET inverter (a) on the output resistance R_{out} and (b) on the input resistance R_{in}.

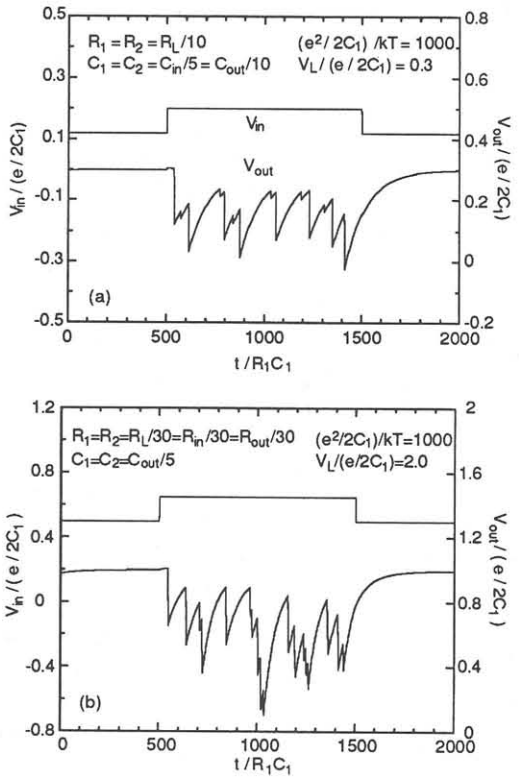

Fig. 5 Switching waveforms of the input and output node voltages of (a) the C-SET inverter and (b) the R-SET inverter.

with the stochastic tunneling events of single electrons. By taking an ensemble average of the output waveform, we can derive a delay time of the inverters. In the case of the C-SET inverter, a pull-up time constant is estimated to be $\tau_{CU} \sim R_L C_{out}$ which is a re-charging time of the charge on C_{out} through R_L, and a pull-down time constant $\tau_{CD} \sim R_d C_{out}$ where R_d is a dynamic resistance of the SET transistor which depends on the input voltage V_{in}. For the R-SET inverter, a pull-up time constant is represented as $\tau_{RU} \sim (R_L // R_{out}) C_{out}$. A pull-down delay $\tau_{RD} = \tau_{RDt} + \tau_{RDr}$ consists of two part: one is turn-on delay $\tau_{RDt} \sim R_{in} C_2$ and the other is rising time constant $\tau_{RDr} \sim R_d C_{out}$. Using the circuit parameters in Fig.5, we determine a switching time τ_s which is a time when the output voltage variation reaches 90% of the logic level difference ΔV_{out}. For the C-SET inverter, we obtain $\tau_{sCU} \sim 250 R_1 C_1$ and $\tau_{sCD} \sim 100 R_1 C_1$, and for the R-SET inverter $\tau_{sRU} \sim 200 R_1 C_1$ and $\tau_{sRD} \sim 150 R_1 C_1$.

As noted above, the output voltage is very oscillational, which seems to cause some problems in stability of the logic operation. A larger output capacitance can stabilize the voltage oscillation, but it lowers the voltage gain and reduces the operating speed. The calculation on transfer characteristics of two cascaded SET inverters indicates that voltage gains larger than unity are obtained in the both inverters, but that input-output separation of the voltage signal is not enough due to the low voltage gain in the case of C-SET inverter.

5.Conclusions

We made simulation study on basic characteristics of the capacitively and the resistively coupled SET inverters in digital logic operation. The calculation of input-output transfer characteristics and dynamic characteristics is made using the semi-classical model by the Monte Carlo method. Although a voltage gain larger than unity is found even in a cascade connection, some disadvantages are revealed such as small voltage gain, poor input-output separation, small logic level difference, instability of operating point depending on the external circuit parameters, and oscillational output voltages, are revealed.

References

1) D. V. Averin and K. K. Likharev, *Mesoscopic Phenomena in Solids*, edited by B. L. Altshuler, P. A. Lee and R. A. Webb, P. 173 (North-Holand, Amsterdam, 1991).
2) J. R. Tucker, J. Appl. Phys. **72** (1992) 4399.
3) L. G. Geeligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina and M. H. Devoret, Phys. Rev. Lett. **64** (1990) 2691.
4) H. Pothier, P. Lafarge, C. Urbina, D. Esteve and M. H. Denoret, Europhys. Lett. **17** (1992) 249.
5) K. Mullen, E. Ben-Jacob, R. C. Jaklevic and Z. Schuss, Phys. Rev. **B37** (1988) 98.