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Low Temperature and Facet-Free Epitaxial Silicon Growth by Contamination-Restrained Load-Lock LPCVD System

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The Si epitaxial growth layer on active region was selectively formed under the low temperature condition from 550 to 620°C without conventional SEG and UHV-CVD system. This technology was achieved using the low temperature "contamination-restrained Load-Lock LPCVD" system and selective etching. The full-flat elevated source/drain (E-S/D) structure was realized on the condition of deposition at 600°C and additional rapid thermal annealing (RTA) at 1000°C in N_2 for 30sec.

1. INTRODUCTION

The need for the formation of ultra shallow junctions in transistor S/D is increasingly enhanced to prevent the short channel effect in future deep submicron ULSI. To attain this purpose, elevated source/drain (E-S/D) structures have been proposed[1)-2)]. Selective epitaxial growth (SEG)[3)-5)] and an ultrahigh vacuum (UHV) CVD[5)-6)] techniques are one of the most promising candidate to form this structure. In the conventional SEG system, epitaxial Si (epi-Si) growth process has been employed a high temperature condition of above 850°C, and a high temperature pre-deposition annealing (above 1000°C) has been used to deoxidize a natural oxide using a large amount of H_2 gas. Therefore, the machine dimension of SEG system becomes very large because of the necessity of a H_2 exhaust gas treatment system. Furthermore, it is difficult to control faceting in the SEG-S/D edges. The facet obstructs the formation of shallow junctions.

In order to realize the full-flat facet-free E-S/D structure, we developed a novel epi-Si growth technique without a H_2 gas and UHV-CVD by using the "contamination-restrained Load-Lock (L/L) LPCVD" system.

2. EXPERIMENTAL

Figure 1 shows the cross-sectional schematics for novel fabrication procedure of E-S/D structure. Using the contamination-restrained L/L LPCVD system, an epi-Si layer on active region and an amorphous (a-Si) or poly-Si layer on SiO_2 region were deposited. Subsequently, selective etching for the a-Si or poly-Si layer was performed by HNO_3, CH_3COOH and HF-based solution. Figure 2 shows the "contamination-restrained Load-Lock LPCVD" system used in this study. Wafers in this system are always kept in the flow of a N_2 gas with the dew point of below -100°C. A wafer was loaded from L/L chamber into the furnace at the temperature range from 550 to 620°C with N_2 flow. The reactor was exhausted by only an oil-free pump. The base pressure is about 0.1 Pa. The epi-Si on active region and a-Si or poly-Si on SiO_2 region were deposited using only SiH_4 gas.

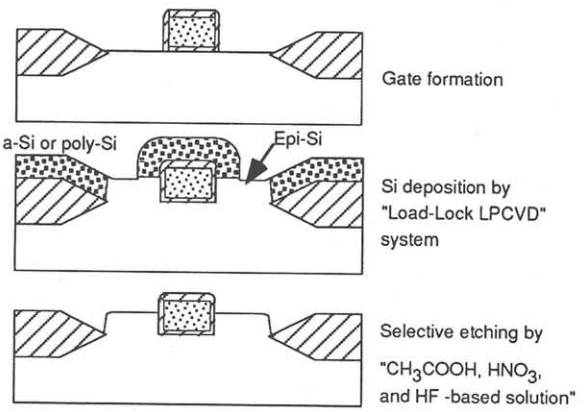

Fig.1 Fabrication procedure of elevated source/drain structure

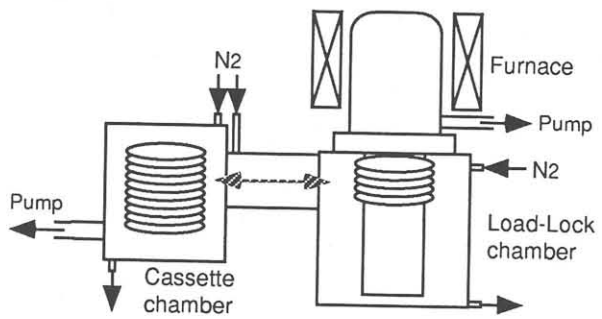

Fig.2 Schematic diagram of the novel "contamination-restrained Load-Lock LPCVD" system

3. RESULTS AND DISCUSSION

Figure 3 shows SIMS depth profiles of oxygen ion for the Si films on the Si substrate deposited by conventional LPCVD and L/L LPCVD systems. The oxygen concentration in the epi-Si layer was very low and native oxide growth on Si surface was suppressed by the L/L LPCVD system. In the epi-Si growth process, a surface cleaning of active region was very important. Especially, the damage-free gate spacer etching was a key technology for this process. When the Si surface was damaged, a furnace annealing or an oxidation to recover the damaged layer was necessary. The additional furnace annealing or oxidation is undesirable in transistor fabrication after ion implantation for controlling the threshold voltage. Furthermore, the oxidation has a serious problem of forming a gate-bird's-beak. In this work, the epi-Si growth was achieved with only conventional pre-deposition HF treatment thanks to the damage-free etching.

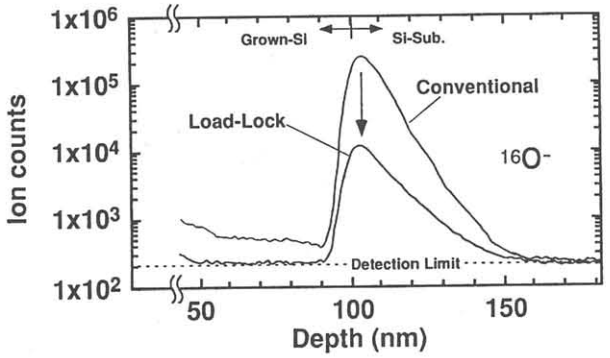

Fig.3 SIMS depth profiles of oxygen ion for the Si films on the Si substrate deposited by conventional LPCVD and L/L LPCVD systems

Figure 4 shows an oblique-directional SEM micrograph of Si layer deposited by L/L LPCVD system at 620°C. By using this system, the epi-Si layer was able to grow on S/D regions. However, it was observed the facets at the gate spacer edges after selective etching, as shown in Fig.5. In order to fabricate the full-flat E-S/D structure, a growth mechanism of epi-Si around the gate spacer was investigated by changing the deposition temperature. Figure 6 shows the cross-sectional SEM micrographs of Si layers deposited from 550 to 620°C. In order to clear the boundary between a-Si or poly-Si and epi-Si layers, a cross section of each sample was etched lightly by delineation etchant. The states of Si films on the SiO_2, at gate spacer edge and on Si regions at each temperature were shown in Fig.7. At the temperature range from 550 to 570°C, the a-Si was deposited on SiO_2 region, and a mono-crystalline Si grew epitaxialy on active region. In the gate spacer area, the epi-Si grew laterally over the gate spacer.

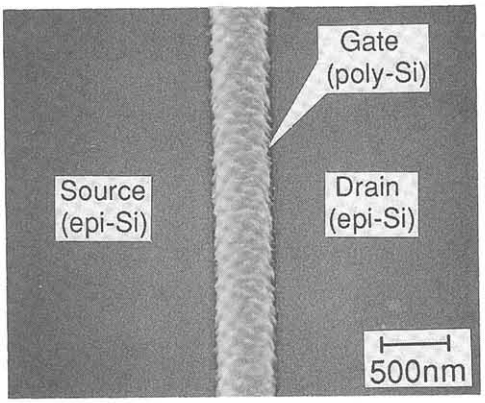

Fig.4 Oblique-directional SEM micrograph of Si layer deposited at 620°C using L/L LPCVD system

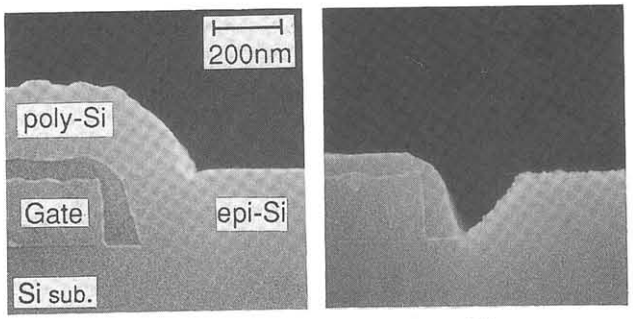

Fig.5 Cross-sectional SEM micrographs of Si layer deposited at 620°C (a) before and (b) after selective etching

However, an issue of faceting was not solved. At the temperature of 580°C which is a critical temperature to change from a-Si to poly-Si on SiO_2, a subgrain boundary was observed between the region "a" and "b" in the gate spacer area. At the temperature range from 590 to 620°C, a poly-Si was deposited on SiO_2 region, and a mono-crystalline Si grew epitaxialy on active region. In the gate spacer area, epi-Si did not grow laterally due to the growth of thermally stable poly-Si. However, triangle region "c" was observed instead of the lateral overgrowth region of epi-Si. In particular, the region "c" with high delineation etching rate was clearly observed at 600°C. It is considered that the formation of region "c" strongly concerns with the stress from poly-Si and epi-Si layers.

If the region "c" changes into the mono-crystalline Si, the E-S/D can be realized as a full-flat. Figure 8 shows the cross sectional SEM micrograph of selective etched Si sample deposited at 600°C and subsequent RTA at 1000°C in N_2 for 30sec. It is confirmed that the region "c" grew into mono-crystalline Si epitaxially and a subgrain boundary was observed at the bottom of the initial triangle region "c". By using the additional RTA, a facet-free full-flat E-S/D was realized.

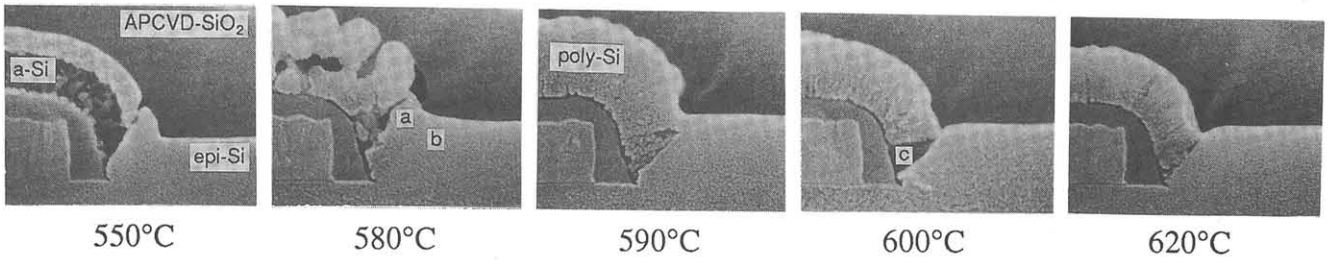

Fig.6 Cross-sectional SEM micrographs of Si layer deposited at various temperatures

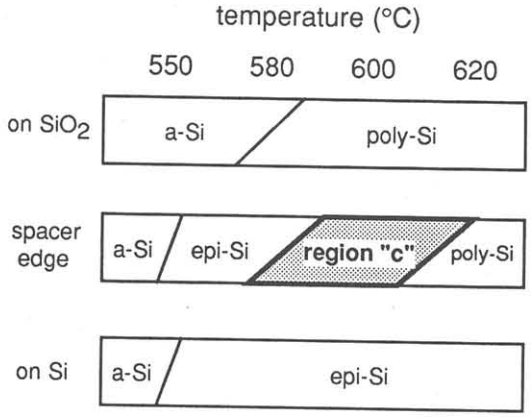

Fig.7 States of Si films deposited at various temperature on each position

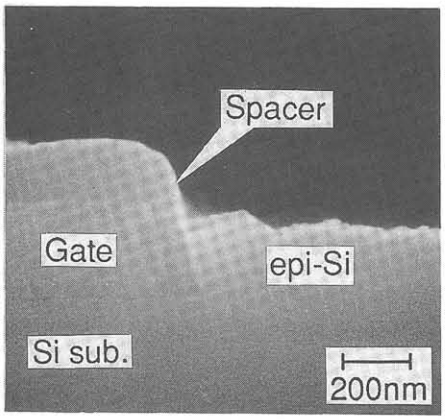

Fig.8 Cross-sectional SEM micrograph of Si layer after selective etching

Figure 9 shows a model of the formation mechanism for the facet-free full-flat E-S/D. This structure was obtained by the Si deposition at 600°C and the additional RTA. The etch rate of region "c" was a very high in delineation etching. From this result, it seems that this region consists of amorphous-like microcrystalline Si. By performing the additional RTA, it is considered that the metastable region "c" changes a mono-crystalline Si easily and a poly-Si layer can not changes a mono-crystalline Si .

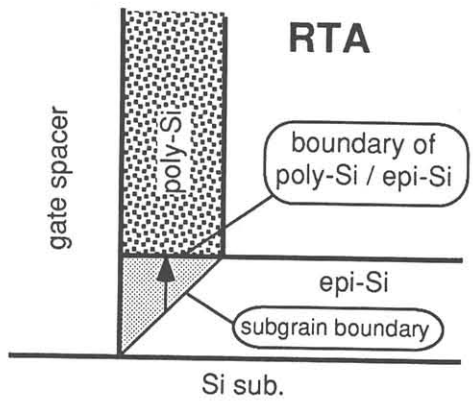

Fig.9 Model of the formation mechanism for the facet-free full-flat elevated S/D

4. CONCLUSION

By using the "contamination-restrained Load-Lock LPCVD" system and subsequent selective etching technique with HNO_3, CH_3COOH and HF-based solution, a Si epitaxial growth layer on the active region was formed selectively without SEG system. Furthermore, the facet-free full-flat elevated S/D structure was formed by the deposition at 600°C and additional RTA at 1000°C. This method can be expected to become important for the development of future deep submicron devices.

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