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Suppression of Leakage Current in Polysilicon NMOS Thin Film Transistors Using NH_3 Annealing

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The effect of NH_3 annealing on polysilicon thin-film transistors (poly-Si TFT) is investigated. Remarkable reduction of the off-state leakage current in self-aligned poly-Si NMOS TFT's is achieved by NH_3 annealing without degradation of on-state characteristics. NH_3 annealing is believed to generate positive fixed charges in the gate oxide near source and drain junction during NH_3 annealing. This positive fixed oxide charges reduce the electric field in the drain junction, resulting in the reduction of the leakage current. The NH_3 annealing can be applied effectively to fabricate high performance self-aligned poly-Si TFT.

1. Introduction

Polysilicon TFT's are used as switching devices in active matrix liquid crystal displays and also as load devices in static random access memories. In order to reduce the loss of stored data in active matrix liquid crystal displays and to reduce the standby power of static random access memories, the leakage current of TFT's should be lowered. However, there are a large number of trap states in poly-Si film which generate large off-state leakage current especially under high applied voltages. There are many techniques to reduce the leakage current in polysilicon TFT's. One effective method is to suppress electric field in the drain junction using the drain offset structure.[1] However, the added series resistance of the ungated channel portion considerably reduces the on-state current. The series resistance problem can be alleviated by doping the offset region lightly[2] or by generating fixed oxide charge in the offset region.[3, 4] These methods require at least an additional lithography step and still have the problem of reducing the on-state current. We propose a new method to reduce the leakage current, while maintaining the on-state current in self-aligned poly-Si NMOS TFT's.

2. Experiment

The schematic main fabrication steps of NH_3 annealed devices are shown in Fig. 1. The detailed fabrication processes of the poly-Si TFT's are as follows. Amorphous silicon films of 1000Å thickness are deposited on thermally oxidized silicon wafers by low pressure chemical vapor deposition system using SiH_4 source gas at 550°C. The wafers are then annealed at 600°C for 48 hours in an N_2 ambient to crystallize the a-Si film. After defining the active regions, 900Å gate oxide is deposited by low pressure chemical vapor deposition at 470°C. Polysilicon film with 4000Å thickness is deposited at 580°C for the gate electrode and is doped with phosphorus using solid diffusion source (PH-1000N) at 970°C for 30 min. After patterning the gate poly-Si film, NH_3 annealing is performed at 650°C, 800°C, 950°C, 1100°C for 30 min in a conventional furnace. The annealing time at 800°C is varied between 15 min and 3 hours. For comparison, TFT's with no annealing (control sample A) and TFT's with simple N_2 annealing at 1100°C for 30min (control sample B) have also been fabricated. Then, the source and drain regions are implanted by phosphorus ion with a dose of 4×10^{15} cm^{-2} at 40KeV for n-channel devices. For p-channel

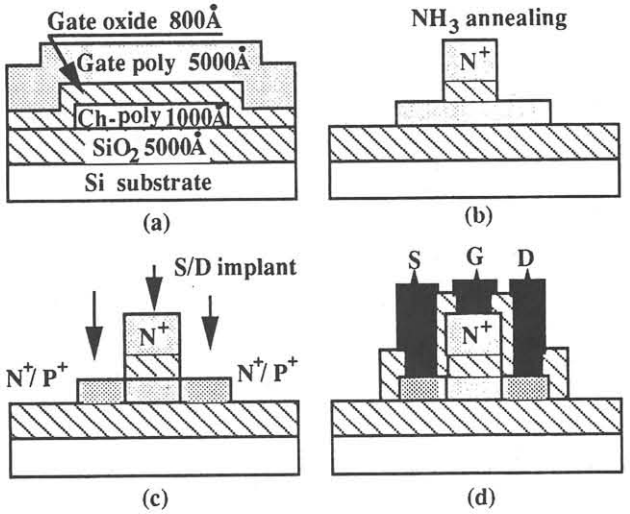


Fig. 1 The main fabrication steps of NH_3 annealed devices. a) gate poly doping using solid diffusion source (970 °C, 30 min) b) NH_3 annealing in conventional furnace c) N^+, P^+ S/D implant d) final device structure (NMOS, PMOS)

devices, BF_2 ion implantation with a dose of $3\times10^{15}cm^{-2}$ at 50KeV is employed. The dopant activation is carried out at 600°C for 24 hours in N_2 ambient. Then, low pressure chemical vapor deposition oxide is deposited as a capping layer and densified at 600°C for 24 hours in an N_2 ambient. After opening the contact hole, Al is deposited and patterned. Finally, all the wafers are alloyed at 450°C for 30 min in an N_2/H_2 ambient.

3 Results and Discussion

Fig. 2(a) compares typical I_D-V_G characteristics of two kinds of fabricated NMOS TFT's, one annealed with NH_3 at 800°C for 30 min, and the other with no annealing (control sample A). The TFT's with NH_3 annealing show lower minimum leakage current by about a factor of 10 at V_D=10V while maintaining almost the same on-state characteristics with a slight lowering of the threshold voltage.

There are three possible mechanisms for the reduction of the leakage current in the poly-Si TFT's with NH_3 annealing. There are : (a) hydrogen passivation in the active channel by decomposition of NH_3 during NH_3 annealing. (b) reduction of the number of defect states by thermal annealing itself at 800°C for 30min during NH_3 annealing. (c) suppression of field by localized fixed charge in the gate oxide near source/drain

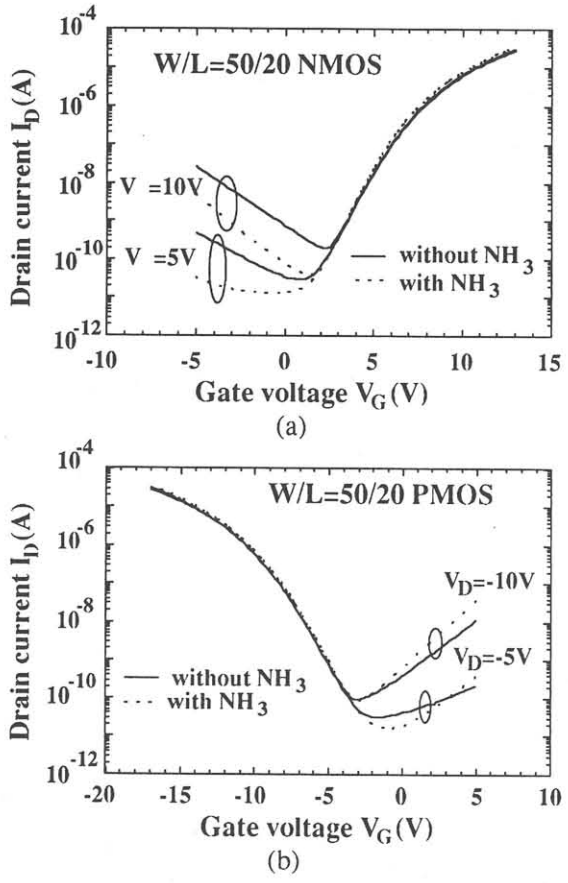


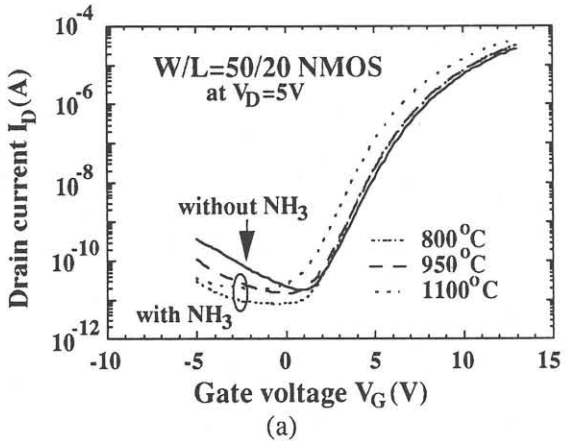
Fig. 2 The I_D-V_G characteristics of TFT's with NH_3 annealing at 800°C for 30 min and without NH_3 annealing, respectively.
(a) NMOS TFT at V_D= 5V, 10V
(b) PMOS TFT at V_D= -5V, -10V

junction due to NH_3 annealing. Since NH_3 annealing is followed by N_2 annealing at 600°C for 24 hours for dopant activation of source/drain and the temperature and time are enough for the outdiffusion of hydrogen in the poly-Si film,[5] the hydrogen passivation is not likely the main cause of the low leakage current. Also, it has been found that TFT's with only N_2 annealing at 1100°C for 30 min (control sample B, not shown in Fig. 1(a)) have higher leakage current than those with NH_3 annealing at 800°C for 30 min. This indicates that the second possible mechanism is not a major cause. Generally, if only the thermal annealing effect is considered, TFT's with higher temperature processing have lower leakage current than those with lower temperature processing.

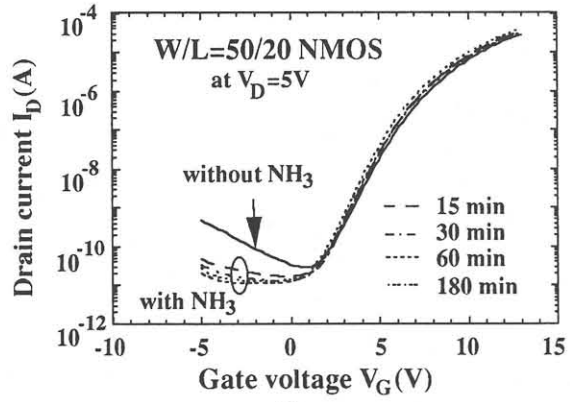
The anomalous leakage current in poly-Si TFT's is known to be due to the field emission via grain boundary traps in the depletion region at the drain junction.[6] The reduction of peak field in the drain junction reduces significantly the leakage current. Previous works[3] have shown that PMOS poly-Si TFT's having negative fixed charge in the offset region have lower leakage current due to the suppression of field. It was also reported that NH_3 annealing generates positive fixed charge in the gate oxide under adequate conditions.[7,8] Furthermore, as shown in Fig. 2(b), in contrary to the characteristics of NMOS TFT's, the leakage current of PMOS TFT's with NH_3 annealing at 800°C for 30 min at high positive V_G is slightly larger than those without NH_3 annealing. This strongly suggests that there is an increase of field in the drain junction by positive fixed oxide charge. At low V_G, where the field effect is negligible, in contrary to the characteristics of leakage current at high V_G, PMOS TFT's with NH_3 annealing have lower leakage current than those without NH_3 annealing due to the reduction of trap states by thermal annealing. From the above, we can infer that NH_3 annealing generates localized positive fixed charge near the source/drain junction, suppresses the electric field from the gate in the drain junction and finally reduces the leakage current in the NMOS poly-Si TFT's. The slight enhancement of on-state characteristics for NMOS and PMOS TFT's with NH_3 annealing shown in Fig. 1 is thought to be caused by the reduction of defect states in the channel poly-Si and the interface of Si/SiO_2 by thermal annealing during NH_3 treatment at 800°C for 30 min.

Fig. 3(a) shows the dependence of leakage current on annealing temperature for a fixed time of 30 min. The I_D-V_G characteristics are not hardly affected by 650°C NH_3 annealing, while the annealing temperature of 800°C is most effective in the reduction of the leakage current. Fig. 3(b) shows the I_D-V_G characteristics of the NMOS TFT's at V_D=5V which is annealed with NH_3 at 800°C for times varying from 15 min to 3 hours. Leakage current decreases by a large amount during the first 15 min and the reduction of the leakage current nearly saturates after 30 min. From the above experimental results, it can be inferred that 800°C annealing is more effective in generating the fixed oxide charge in CVD oxide than higher temperature annealing and that the value of fixed oxide charge generated by NH_3 annealing at 800°C in densified CVD oxide is nearly saturated for 30 min NH_3 annealing.

The activation energies of the drain current are shown in Fig. 4. The activation energy of the off-state



(a)



(b)

Fig. 3 The I_D-V_G characteristics of NMOS TFT's with and without NH_3 annealing at a drain voltage V_D=5V.
a) for varying annealing temperature ranging from 800 °C to 1100 °C at a fixed time of 30 min
b) for varying annealing time ranging from 15 min to 180 min at a fixed temperature of 800 °C

regime increases after NH_3 annealing and becomes about half the bandgap energy, which implies that the leakage current is caused mainly by thermal activation and that the field induced process is suppressed. It is believed that the positive fixed charges at the drain junction suppress and shield electric field from the gate and reduces the leakage current.

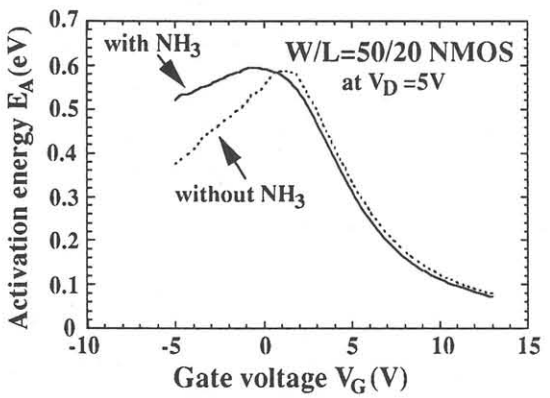


Fig. 4 Activation energy variations with gate voltage for the devices with NH_3 annealing at 800 °C for 30 min and without NH_3 annealing.
Devices are measured at V_D= 5V in the temperature range of 20 °C to 100 °C.

4. Conclusions

Remarkable improvement of the leakage current in NMOS poly-Si TFT's has been achieved by NH_3 annealing without degradation of on-state characteristics. It is believed that NH_3 annealing generates the positive fixed charges in the gate oxide near the source and drain junction and the positive fixed charges suppress the electric field in the drain junction, thus resulting in the reduction of the leakage current. Finally, it has to be noted that the generation of the positive fixed charges in oxide near the source and drain junction described here is a self-aligned scheme.

5. References

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