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20% Reduction Both of Cell Area and of Mask Layers in Simplified TFT-SRAM Process

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Cell area and mask steps of 16Mb TFT-SRAM were reduced about 20% compared with our previous work. A 6.6μm2 cell area was realized with suitable memory cell layout for modified illumination lithography, and Self-Aligned-Contact (SAC) with As implanted Load-Lock-LPCVD polysilicon, based on minimum dimension of 0.35μm. And 20% reduction of mask steps was realized by high energy implantation for CMOS process, and highly selective contact etching technique.

Introduction

In the development of high density SRAMs, as the memory cell size and supply voltage reduction, ensuring the high cell stability is one of the important issue. Recentry, several memory cells have been reported to obtain the high stability, such as a split word line cell [1][2][3], or a cell with strage node capacitor.[2][4]

On the other hand, increasing of process steps and process complexity of TFT-SRAM cell has been becoming the another majour issue. These increase cause an increase of the chip cost, and pull down a competitive power of SRAMs with other memories, such as Pseudo SRAMs. In this work, we realized a 16Mb TFT-SRAM cell whose cell area and mask steps were reduced about 20% compared with our previous work. (5)

We have adopted a new cell layout which is so suited to the modified illumination lithography that DOF is increased more than 1μm. And Self-Aligned-Contact (SAC) technology also served for memory cell size reduction. A Load-Lock-LPCVD Polysilicon(L/L-Poly) and As implantation for polysilicon doping are the key technologies to reduce the contact resistance without degrading the short channel effect of cell transistors. These technologies achieved memory cell area of 6.6μm^2, which was about 80% of the previous cell, based on minimum dimension of 0.35μm..

We have simplified CMOS process using high energy implantation and decreased contact etching steps using highly selective contact etching technique. These technologies realize a SRAM process whose mask steps is about 20% less than the previous one.

Therefore, this technology is a promising candidate for the high density SRAM such as 16M and beyond.

Process technology

In a TFT-SRAM process, delineation of NMOS gate electrodes is a key process step which determines cell size. Levenson type phase-shift mask has a possibility to realize a fine pattern formation overcoming the limitation of i-line normal illumination (6). But this technique has severe problems in a mask fabrication, and for this reason, application to mass production may be difficult. Modified illumination is the another candidate for future VLSI and is adequate for mass production (7) because this technique needs no special technology for mask fabrication. However, since this technique is only effective for repeating line patterns, we layouted all the NMOS gate electrodes of a new SRAM cell in parallel as shown in Fig.1.

By adopting this layout, 2.2x3.0μm^2 cell size is obtained, and this value is about 20% less than our old cell. The depth of focus(DOF) is 1.0μm for the modified illumination stepper, while the DOF is only 0.2μm for the conventional illumination.

A cross sectional SEM view of this cell parallel to bit-line is shown in Fig.2. The first WSix polycide layer is used as gate electrodes; the second WSix polycide is deposited on SACs and acts the ground line and the bit line contact pads; the third poly-Si forms the TFT gate electrode. This poly-Si connects the PMOS load TFT and the storage node through a contact that is opened both on a drain of driver transistor and gate electrode of another driver transistor. The forth thin poly-Si layer serves as the TFT body and Vcc line.

For contact hole formation, we introduced Inductive Coupled Plasma Etching Technique. Since the selectivity of SiO2 to Si in this technique is more than 50, contact

holes which have different contact depth can be etched at one time. Therefore, resist layers for the contact hole opening are reduced to only one from three compared with the old process. Tungsten plugs are adopted for contact holes and via holes.

Simple CMOS process

In Fig.3, the schematic view of simple CMOS process flow are shown. In this process, well implantations, Vth adjustment implantations and channel stop implantations are done with only two photolithographic steps, while three or four resist masks have been used for the conventional CMOS process We adapt high energy implantation for twin well formation after LOCOS isolation process. For N-well, phosphorous ions are implanted with the acceleration energy of 600keV and the dosage of $3x10^{13}cm^{-2}$, and for P-well, boron ions are implanted with 250keV,$1x10^{13}cm^{-2}$. The doping profiles of twin well are retro-graded type shallow well, and the depth of peak impurity concentration of N-well is about 1.0μm, and P-well is about 0.6μm respectively.

NMOS FET (W/L=10/0.35μm) & PMOS FET (W/L=10/0.5μm) characteristics are shown in Fig.4. And the current gain (h_{FE}) of the parasitic vertical PNP bipolar transistor that represents a guideline of latch-up destruction, is also evaluated. (Fig,5) The h_{FE} decreases drastically as increase of N-well impurity concentration which acts as the base region of the PNP transistor. All these characteristics represent that this simple CMOS process is applicable for the future VLSI devices such as 16Mb SRAMs.

Short channel effect of SAC structure

In order to decrease the SRAM cell area, SAC is indispensable technique. In this SAC technology, there are two serious problems, and their relationship is an antinomy. One is the native oxide formation at the poly-Si/N+ diffusion interface, which increases a contact resistance. To overcome this problem, we have used the Load-Lock Poly-Si LPCVD system, and obtained a sufficiently low contact resistance.(5) However, preventing the native oxide formation at the interface of SAC, the another problem of the transistor short channel effect.(SCE) becomes more seriously. The dopant of poly-Si diffuses through a SAC without diffusion barrier of native oxide, and enlarges the transistor source/drain diffusion area below the gate electrode. In Fig.6 the dependence of threshold voltage on gate length are shown. Non SAC transistor is excellently suppressed the SCE, on the other hand, the threshold voltages of SAC transistors with the Poly-Si doped by POCl3 diffusion decreases rapidly as gate length decrease. In the same figure, the SAC transistors with Poly-Si doped by ion implantation of Arsenic or Phosphorous are also shown, the dosage of both samples is $6x10^{15}cm^{-2}$. The phosphorous implanted sample shows the same SCE degradation as POCl3 doped sample. On the other hand, because of the diffusion coefficient of arsenic is about one order lower than that of phosphorous, the arsenic implanted sample excellently prevents the SCE degradation, and show the same characteristics as the non-SAC transistor.

Device characteristics

For the driver transistor with a channel length of 0.35μm, a drive current of 0.35mA/μm has been obtained at 3.0V. The Id-Vg characteristics for the TFT with a 20nm gate oxide and a 20nm channel poly is presented in Fig.7. For L/W=0.5/0.4μm device, an OFF current of 30fA and an on-to off ratio of 10^6 have been achieved. These values are considered enough for realizing the 16Mb SRAMs with a stand-by current less than 1μA at 3V. The bit line contact resistance of 170Ω and the grand line contact resistance of 110Ω have been achieved without inducing Vth down of driver & access transistors with SAC structure by Load-Lock Poly and As implantation doping.

By employing these technologies, we fabricated a 128kb SRAM test chip, and we confirmed the normal operation of this chip under a supply voltage of 3V.

Conclusion

A new SRAM process with a small cell area of $6.6\mu m^2$ has been realized. The modified illumination and the SAC structure are key technologies to decrease the cell area. The Load-Lock LPCVD Poly-Si and As implantation achieve low contact resistance and suppression of short channel effect. The simplified process and the highly selective oxide etching reduces number of mask layers to be 80% of the previous one. These technologies are promising for sub-halfmicron SRAM such as 16Mb and beyond.

Acknowledgement

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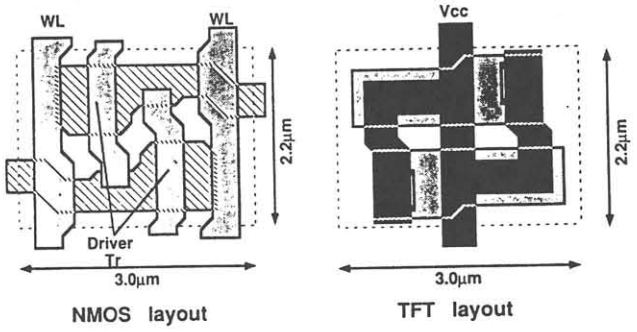

Fig.1 New Memory Cell Layout

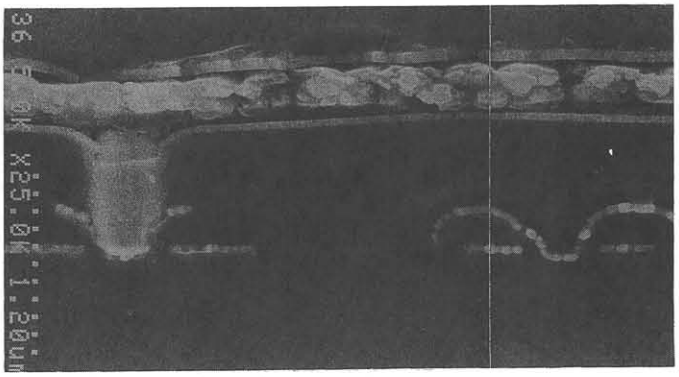

Fig.2 Cross Sectional SEM Photograph of New Memory Cell

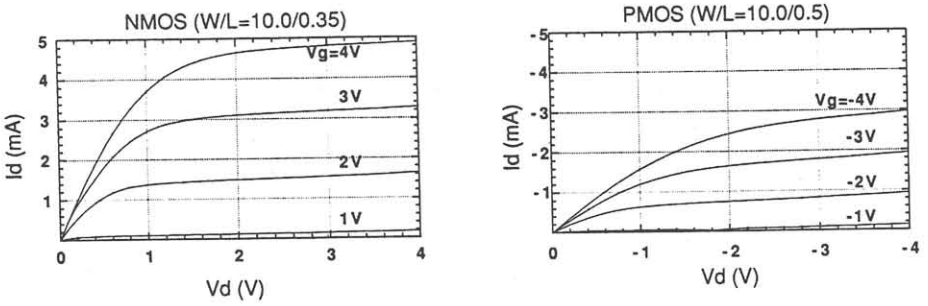

Fig.4 NMOS & PMOS characteristics fabricated with Simple CMOS Process

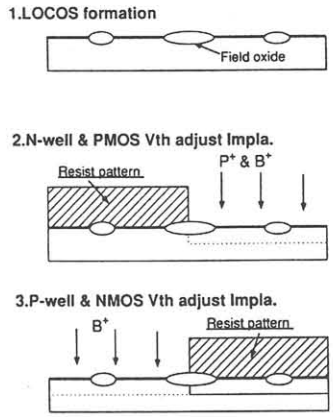

Fig.3 Schematic view of Simple CMOS Process Flow

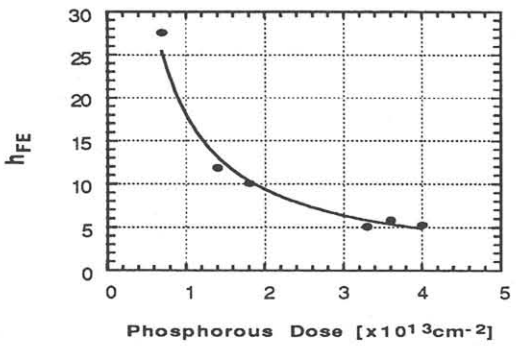

Fig.5 Dependence of h_{FE} of Parasitic PNP Transistor on N-well Dosage

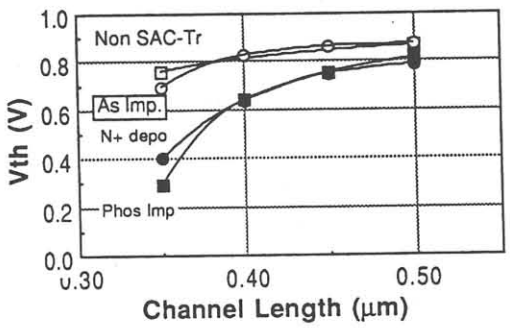

Fig.6 Dependence of Vth on Channel Length of SAC Transistors

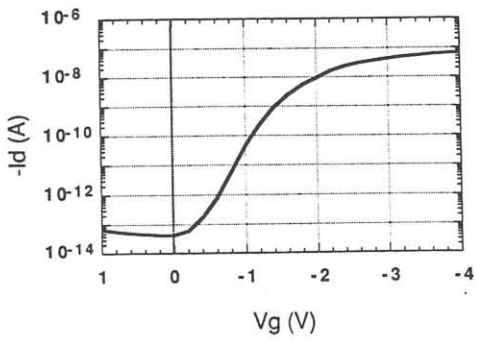

Fig.7 TFT characteristic of Id vs Vg (W/L=0.5/0.6μm, Vd=-3V)