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Dependence of Hot-Carrier Effect on Internal Stress in TiN/Poly-Si Gate MOSFET

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Abstract

The hot-carrier (HC) effect of the TiN/poly-Si gate MOSFET, which is used in dual-gate CMOS to connect n+ and p+ poly-Si gates directly, was studied. The HC lifetime is 1/3 that of conventional poly-Si gate MOSFET, however, it is independent of internal stress. The results suggest the reason for HC lifetime degradation is not tensile stress in this device, but oxide damage at TiN/poly-Si gate edges. By improving dry-etching technique of gate, TiN/poly-Si gate structure promises reliable operation of sub-μm devices.

1. Introduction

The TiN/poly-Si gate MOSFET has previously been developed for use in dual-gate CMOS devices which have an n+ poly-Si gate for nMOS and a p+ poly-Si gate for pMOS FETs [1]. It provides a low-sheet-resistance gate, and miniaturizes cell sizes of fundamental logic gates by connecting n+ and p+ poly-Si gates directly, as shown in Fig. 1. However, TiN causes high internal stress which degrades hot-carrier (HC) lifetime [2] ; therefore the HC effect of this MOSFET should be studied in detail. In this work, we clarify the relationship between the internal stress and HC effect in this device structure, and determine the main reason for HC lifetime degradation.

2. Device structure and Basic characteristics

TiN/poly-Si gate structure, as shown in Fig.1, was fabricated by process sequence described below. After 6nm-gate-oxide and non-doped 100nm-gate-poly-Si were formed, phosphorus and boron ions were implanted to n+/p+ gate region. Next, 100nm-

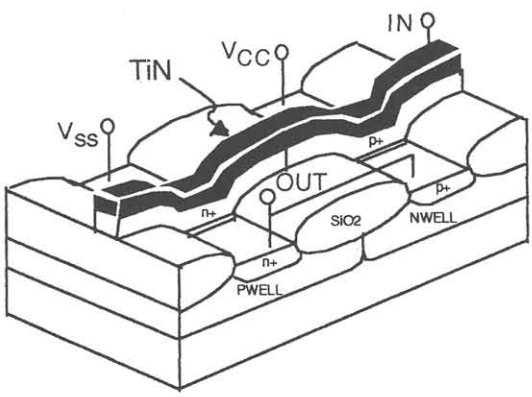

Fig. 1. TiN/poly-Si dual-gate structure (Inverter)

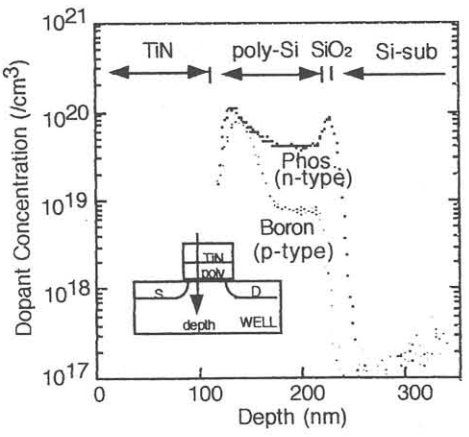

Fig. 2. SIMS profiles in gate poly-Si.

TiN and 100nm-SiO_2 were deposited and patterned by dry-eching, followed by implantation for source/drain. The sheet resistance of this gate was 10 ohm/sq., which agrees well with the value calculated from the material constant. After dielectric layers below metal was deposited, themal annealing of 850℃-10min was performed. SIMS profile in gate poly-Si after this thermal annealing is shown in Fig. 2. Concentrations of both phosphorus and boron ions are about $10^{20}/cm^3$ at TiN/poly-Si interface, and they indicate impurity absorption by TiN is small.

Lateral dopant diffusion is suppressed to sub-μm region, and n+ and p+ poly-Si gates are successfully connected in TiN/poly-Si gate structure as shown in Fig. 3. The test structure in Fig. 3 estimates work function, which depends on dopant concentration in poly-Si by measuring threshold voltage. Threshold voltage shift was less than 0.07 V in TiN/poly-Si gate structure, while it varied from 0.2 to 0.4 V in conventional $TiSi_2$/poly-Si gate structure according to lateral dopant diffusion.

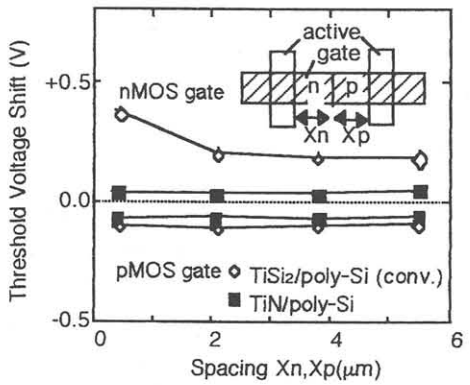

Fig. 3 Dependence of threshold voltage on Xn, Xp; spacing from gate-implant boundary.

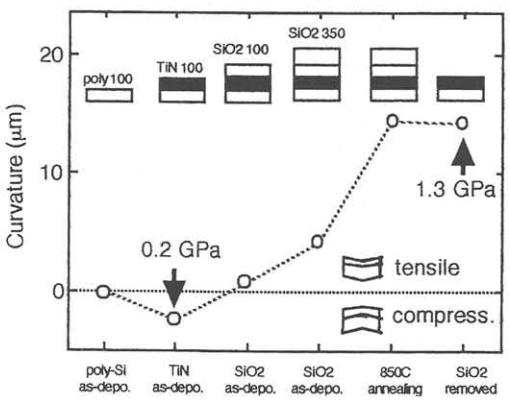

Fig. 4. Curvature of wafer.

3. Internal stress and HC effect

Internal stress is compressive when TiN is deposited, and it changes to tensile after thermal annealing (850℃-10min). It was estimated by curvature of the wafer, as shown in Fig. 4, which was measured with a laser-beam flatness tester. The HC lifetime of the TiN/poly-Si gate MOSFET is about 1/3 that of the poly-Si gate MOSFET as shown in Fig. 5. However, an HC lifetime of 10-years in the TiN/poly-Si gate MOSFET is achieved at 2.3 V which is enough for low-voltage operation below 2 V.

Dependence of HC lifetime on mechanical force is shown in Fig. 6. The mechanical force was changed by gate thickness because mechanical force is directly proportional to gate size and internal stress. HC lifetime of the TiN/poly-Si gate MOSFET is independent of mechanical force, although it is shorter than that of the poly-Si gate MOSFET. These results show that the main reason for HC lifetime degradation is not the tensile stress in the TiN/poly-Si gate MOSFET. This agrees with a previous study which reported that only compressive stress increases interface trap densities and causes the degradation [2]. Gm degradation of MOSFETs which have different gate lengths, Lg, are shown in Fig. 7. The gm degradation of the TiN/poly-Si gate MOSFET is larger than that of the poly-Si gate

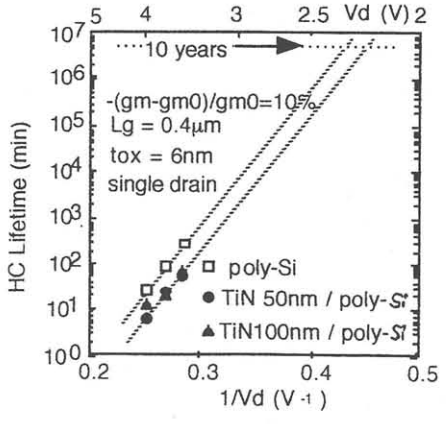

Fig. 5. Dependence of DC hot-carrier lifetime on inverse of Vd.

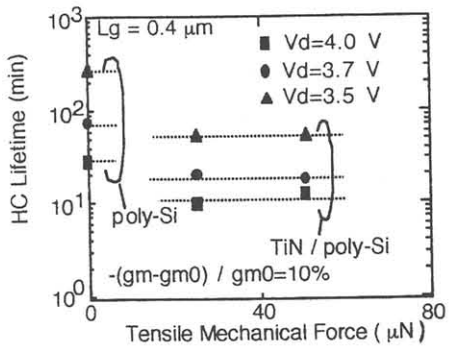

Fig. 6. Dependence of DC hot-carrier lifetime on mechanical force.

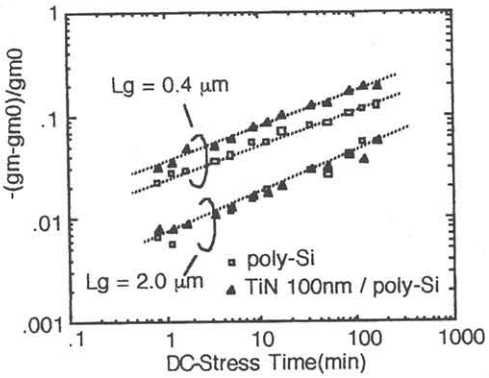

Fig. 7. Dependence of gm-degradation on DC-stress time.

than that of the poly-Si gate MOSFET in 0.4-μm-Lg devices, while they are almost the same in 2.0-μm-Lg devices. This result indicates that internal stress is not the main reason for degradation, because mechanical force in 0.4-μm-Lg devices is smaller than that in 2.0-μm-Lg devices. The gm degradation increases in short-Lg devices in which gate edges have large parts of the channel region. It suggests that the degradation is increased by oxide damage at the gate edges in the dry etching process of the TiN/poly-Si gate.

4. Conclusion

TiN/poly-Si gate MOSFET which provides low-sheet-resistance gate, and enables to connect n+ and p+ poly-Si gates in dual-gate CMOS directly, have been fabricated. Although the HC lifetime of this MOSFET is about 1/3 that of the conventional poly-Si gate MOSFET, it is independent of internal stress because the internal stress caused by TiN is tensile. Our experimental results suggest that the oxide damage at the gate edges degrades the HC lifetime, and TiN/poly-Si gate structure promises reliable operation of sub-μm devices by improving dry-etching process technique.

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