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Impact of Source-Drain Extension Dose on Hot-Carrier Reliability in 0.1μm nMOSFETs

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In this paper, the hot-carrier reliability and performance of source-drain extended nMOSFETs fabricated with various source-drain extension doses are discussed. It is shown the nMOSFET with an optimum dose of $1\times10^{15}cm^{-2}$ has higher reliability and performance, compared to the LDD nMOSFET. Moreover, the influence of the hot-carrier degradation on circuit speed is examined by circuit simulation, and the advantage of the source-drain extended nMOSFETs is discussed from the viewpoint of both reliability and performance.

1. INTRODUCTION

Using a shallow source-drain extension(S/D-ex) in combination with deeper source and drain is one of the most important factors to increase current drivability and reduce short channel effects in 0.1μm MOSFETs[1]. However, one of the concerns for the source-drain extended nMOSFETs is the hot-carrier reliability, since the electric field near the drain region is not fully relaxed because of high-doped source-drain extension, compared to conventional LDD nMOSFETs. In this paper, we studied the hot-carrier reliability of nMOSFETs fabricated with different source-drain extensions doses and the electric field distribution near the drain region in device simulation, and investigated differences in degradation between the LDD and the source-drain extended nMOSFETs. Moreover, we examined the influence of the hot-carrier degradation on circuit speed by circuit simulation, and discussed the advantage of the source-drain extended nMOSFETs from the viewpoint of both reliability and performance.

2. DEVICE FABRICATION

Figure 1 shows a schematic cross-section of the source-drain extended nMOSFET. After the channel region was implanted by B^+ 30keV with a dose of $6\times10^{12}cm^{-2}$, the gate electrode on a 4nm-thick gate oxide was patterned by electron beam lithography. The source-drain extensions were implanted by As^+ 10keV with various doses from 1×10^{14} to $1\times10^{15}cm^{-2}$, and 60nm-thick SiO_2 sidewall was fabricated. After RTA at 1000℃ for 10 seconds, the source-drain extended nMOSFETs with an effective channel length of 0.16μm were fabricated. Conventional LDD

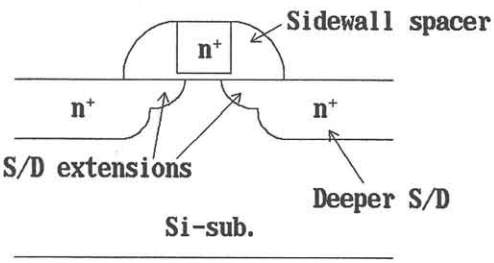


Fig.1 Schematic cross-section of source-drain extended (S/D-ex)nMOSFET

nMOSFETs were also fabricated by As^+ 10keV implantation with a dose of $1\times10^{13}cm^{-2}$ as controls. The impurity concentration in the LDD is larger than that in the channel region by a factor of 10, and a depletion layer is formed in both channel and drain regions. With a dose over $1\times10^{14}cm^{-2}$, the depletion layer is scarcely formed in the drain region, and we call the source-drain fabricated with a dose of $1\times10^{13}cm^{-2}$ as LDD and that with a dose over $1\times10^{14}cm^{-2}$ as extended source-drain, in this paper.

3. EXPERIMENTAL RESULTS AND DISCUSSION

As shown in Fig. 2, the drain current of the source-drain extended nMOSFETs increases with dose, and is higher than that of the LDD nMOSFET by 40% for a channel length of 0.16μm and a dose of $1\times10^{15}cm^{-2}$. The hot-carrier lifetime both for the LDD and the source-drain extended nMOSFETs for a channel length of 0.16 μm was measured under DC stress, as shown in

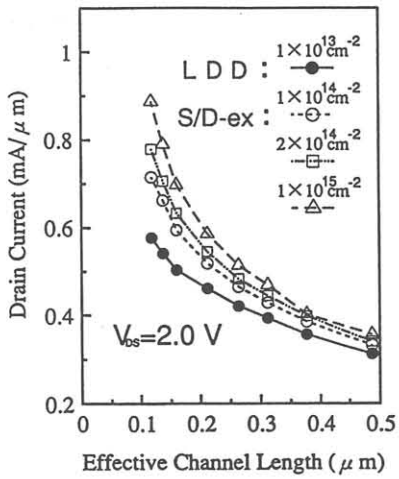


Fig. 2 Gate length dependence of drain current with various doses

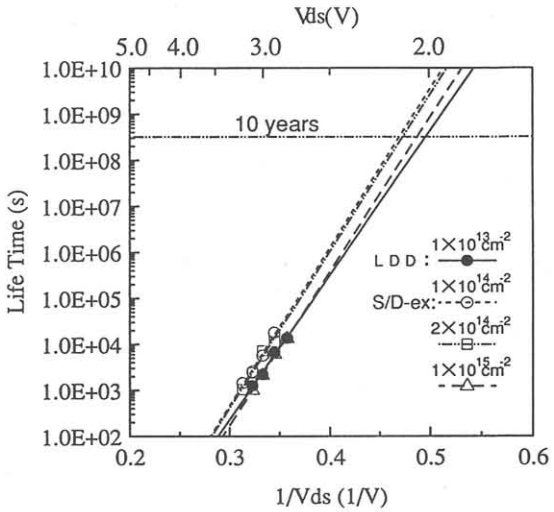


Fig. 3 Lifetime dependence of drain voltage with various doses

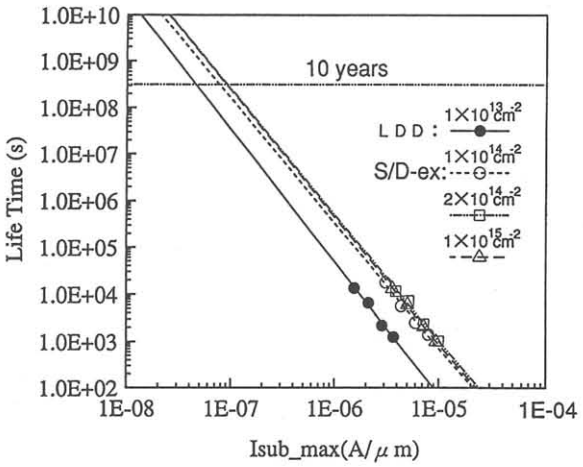


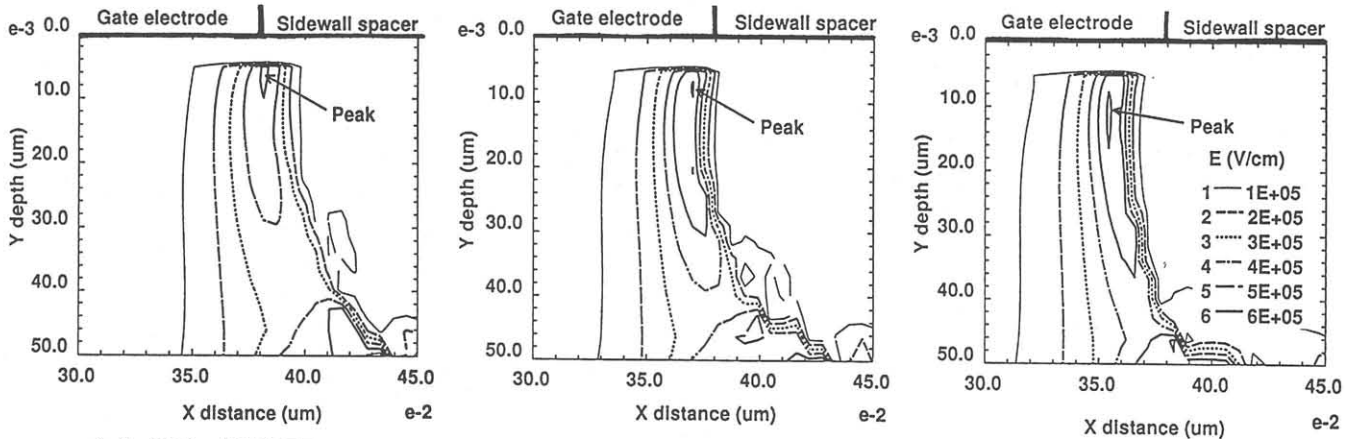
Fig. 4 Lifetime dependence of substrate current with various doses

Fig. 3 and 4. A stress gate voltage was chosen for maximum substrate current, and the lifetime was defined as a stress time for 10% degradation of the drain current. The drain current was measured in reverse mode after stress. Under a dose of $1\times10^{15}cm^{-2}$, the source-drain extended nMOSFETs show longer lifetime than the LDD nMOSFET, as shown in Fig. 3. For the same substrate current, the source-drain extended nMOSFETs' lifetime is longer than the LDD's by a factor of 10, and there is no significant difference in degradation between the source-drain extended nMOSFETs with different doses, as shown in Fig. 4.

Electric field distribution parallel to a current path was simulated near the drain region at a drain voltage of 2.0 V to investigate the hot-carrier phenomena, as shown in Fig. 5. Hot carriers are considered to generate near the peak. In the LDD nMOSFETs, hot-carriers injected in the sidewall spacer make the drain region pinch-off under the sidewall spacer and degrade the nMOSFETs[2]. On the other hand, the source-drain extended nMOSFET is degraded not by pinch-off but by hot-carrier injection to the gate oxide, because the peak is shifted from the sidewall edge. Therefore, the threshold voltage shift is larger than that of the LDD under the stress condition with similar degradation of the drain current between the LDD and the source-drain extended nMOSFETs, as shown in Fig. 6.

For the source-drain extended nMOSFETs with increasing the dose, the peak remains under the gate oxide, and shows little difference in depth, and there is no significant difference in the degradation for the same substrate current, as shown in Fig. 5(b) and (c). The lifetime can be estimated only by the dose, and an optimum dose can simply be chosen which gives the source-drain extended nMOSFET both higher current drivability and reliability at the same time, differing from the LDD. At a drain voltage of 2.0V, a dose over $1\times10^{15}cm^{-2}$ makes the substrate current more than $1\times10^{-7}A$ and the source-drain extended nMOSFET's lifetime less than the LDD's(10 years), as shown in Fig. 4 and 7. Therefore, considering the trade-off between the current drivability and the reliability, we can increase the dose up to $1\times10^{15}cm^{-2}$. In conclusion, we have realized nMOSFETs with higher reliability and performance by using a dose of $1\times10^{15}cm^{-2}$.

The source-drain extended nMOSFET showed larger threshold voltage shift caused by the hot-carrier, and we examined the influence of both the shift and the drain current degradation on circuit speed by circuit simulation. Table I shows the shift and the degradation estimated under 10 years' stress at a drain voltage of 2.0V, the simulated delay time degradation of an invertor with a channel



(a) LDD nMOSFET Dose:$1\times10^{13}cm^{-2}$

(b) S/D-ex nMOSFET Dose:$1\times10^{14}cm^{-2}$

(c) S/D-ex nMOSFET Dose:$1\times10^{15}cm^{-2}$

Fig.5 Simulated electric field distribution at V_{DS}=2.0 V

length of 0.16μm, and the delay time ratio before the stress, between the LDD and the source-drain extended(dose:$1\times10^{15}cm^{-2}$) nMOSFETs. The source-drain extended nMOSFET shows no significant difference in the delay time degradation, and improves the delay time over 10%, compared to the LDD. We have demonstrated the advantage of the source-drain extended nMOSFET from the point of both reliability and performance.

4. SUMMARIES

We have studied the hot-carrier reliability of source-drain extended nMOSFETs fabricated with various source-drain extended doses, and realized nMOSFETs with higher reliability and performance by using an optimum dose of 1×10^{15} cm^{-2}, compared to the LDD nMOSFET. Moreover, we have investigated differences in the degradation and the delay time between the LDD and the source-drain extended nMOSFETs by using device and circuit simulations, demonstrating that both higher current drivability and reliability were obtained at the same time for the source-drain extended nMOSFET.

ACKNOWLEDGEMENT

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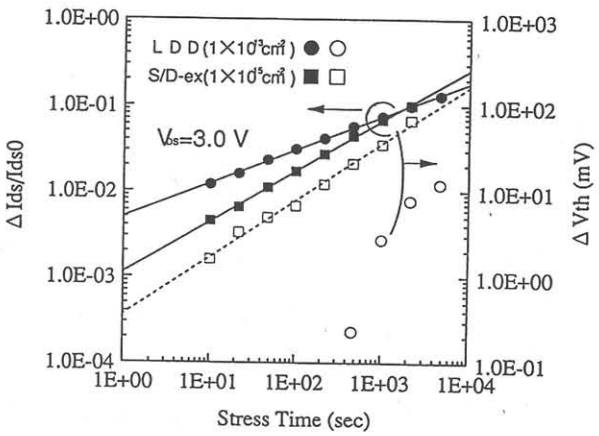

Fig.6 Drain current degradation and threshold voltage shift dependence of stress time between LDD and source-drain extended nMOSFETs

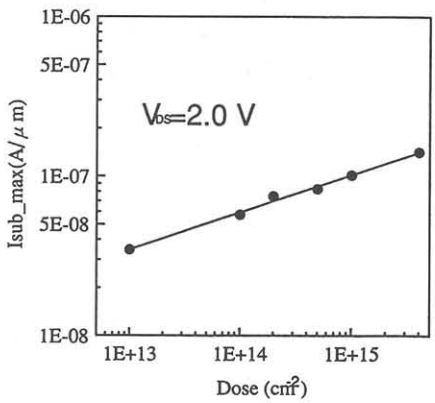

Fig.7 Substrate current dependence of source-drain dose

Table I Comparison of LDD and source-drain extended nMOSFETs

	$\frac{\Delta Ids}{Ids0}$	Δ Vth	$\frac{\Delta tpd}{tpd0}$	$\frac{tpd0(S/D\text{-}ex)}{tpd0(LDD)}$
LDD	10%	7mV	4%	87%
S/D-ex	7.6%	40mV	2%	