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Ultra Short and Narrow Channel Si MOSFETs with Advanced SEG Isolation Fabricated by Ultra High Vacuum CVD

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Selective epitaxial growth by Ultra High Vacuum CVD using pure Si_2H_6 gas was firstly introduced in a Si LSI process, so as to minimize crystallographic defect and "facet". The facet width was 0.03μm, which is consistent with the requirement of device miniaturization and results in possibility of ultra narrow channel MOSFETs. The narrow channel effect was successfully suppressed, and the maximum transconductance reaches 530mS/mm for an ultra short (0.1μm) and narrow (0.3μm) channel N-MOSFET.

1. INTRODUCTION

The scaling trend of Si MOSFETs increasingly improves device performance. A wide variety of MOSFET structures has been proposed for deep sub-micron LSIs. Although, in such studies, some of them have realized 0.1 μm MOS devices, only dimension of the gate electrode (gate length) was scaled down. Very few reports have discussed total miniaturization including device isolation, whereas the scaling of the channel width is also indispensable for low power devices.

For the development of device isolation, Selective Epitaxial Growth (SEG) of silicon was developed for device isolation using Low Pressure (LP) CVD and SiH_2Cl_2 - H_2 - HCl gas system (1), (2), (3), in which Cl atoms etch away silicon nucleus on SiO_2 surface and cover SiO_2 surface to control selectivity (4). However, in such a process, the facets plane grows as fast as the main plane due to the etching of Cl atoms and hence it is impossible to deposit in the narrow active area.

In this paper, a novel ultra short and narrow channel Si MOSFET utilizing SEG has been reported. Ultra High Vacuum (UHV) CVD using pure Si_2H_6 gas (6) has been introduced, in order to limit facets while maintaining selectivity. This process realizes an advanced SEG isolation with a smaller number of process steps compared with LOCOS and trench isolation, while maintaining low leakage current. The gate length and the gate width of MOSFETs can be scaled down to 0.1μm and 0.3μm, respectively.

2. DEVICE FABRICATION

The fabrication step is very simple as shown in Fig.1. A SiO_2 layer of 200nm thick was patterned on the p-type silicon substrate with (100) orientation, and non-doped silicon was selectively grown in the active region at 660 °C. In this case, the epi-growth can be done at the same surface condition for N and P-MOS regions. The epi reactor was water cooled cold-wall UHV -CVD system (ANELVA SRE-612). The back-ground pressure in the growth chamber realized 6X10-^{10}Torr. The source gas was pure Si_2H_6. The gas flow rate was 1.0 sccm. The conventional SEG process utilized chlorinated silanes as Si source or required additional gas such as HCl to control selectivity. However, UHV-CVD realizes selective silicon epitaxy without HCl which promotes to grow the facets plane (4), (5).

Boron ions for N-MOSFETs and phosphorus ions for P-MOSFETs were implanted for a twin well combined with the channel stopper. The implant energies were 150KeV for boron, 360KeV for phosphorus to implant through the isolation oxide. Immediately after 4nm-gate oxide formation, the poly-silicon film for gate electrode was deposited. The source/drain and highly doped gate electrode were simultaneously doped, so that both N-MOSFET and P-MOSFET were surface channel transistors. The conventional bulk MOSFETs with LOCOS isolation were also fabricated by the same process conditions. The LOCOS oxide thickness was 350nm.

The SEM photograph of the 0.1μm poly-silicon gate electrode on the selectively grown silicon and the

isolation oxide is shown in Fig.2. It is clearly observed that highly precise patterning has been achieved due to the perfectly planarized surface between epi-silicon and isolation oxide. The width of facets is approximately 0.02-0.03μm, which makes it possible to fabricate ultra narrow active pattern less than 0.5μm

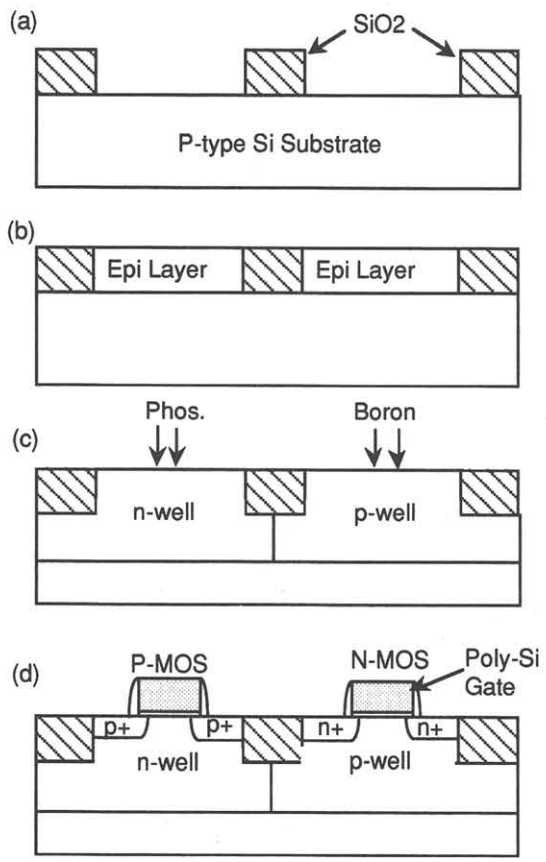

Fig.1 Process sequence of SEG MOSFET.
(a) Silicon oxide was patterned.
(b) Non-doped silicon was selectively grown. (c) Twin well combined with channel stopper was implanted.
(d) MOS transistor was fabricated.

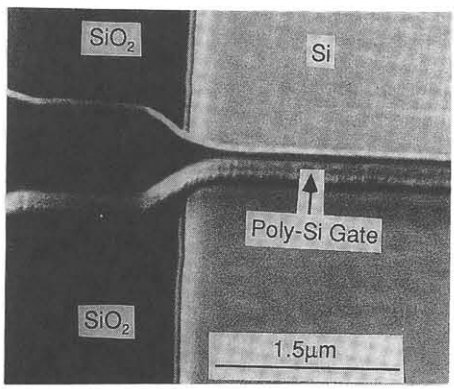

Fig.2 SEM photograph of the surface of epi layer and the 0.1μm gate electrode.

3. RESULTS AND DISCUSSIONS

The leakage currents of the source/drain junction (p-n diode) and the isolation are shown in Fig.3. It is found that the leakage current of SEG MOSFET is compatible with that of the conventional LOCOS MOSFET for both junction and isolation leakage.

Fig.4 shows the subthreshold characteristics of 0.1μm gate length N-MOS and 0.2 μm P-MOS. This results also indicates that no leakage current of SEG MOSFETs was observed. The subthreshold slope is 90mV/dec. for N-MOS and 85mV/dec. for P-MOS.

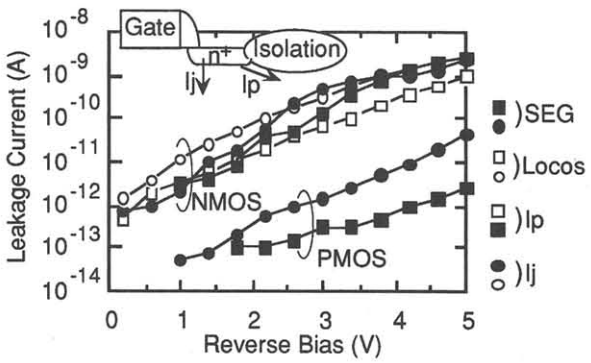

Fig.3 Leakage currents as a function of reverse bias voltage for SEG and conventional LOCOS devices. Isolation length is 3762μm, junction area is 9380μm^2.

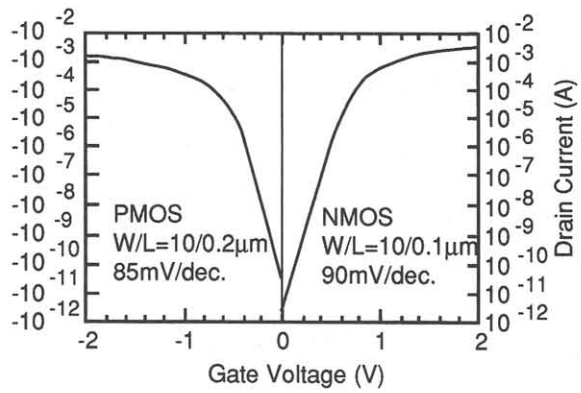

Fig.4 Subthreshold characteristics of SEG N and P-MOSFETs.

The threshold voltage as a function of the gate width (narrow channel effect) was investigated as shown in Fig.5. The narrow channel effect was successfully suppressed and the threshold voltages of N and P-MOSFETs with 0.3μm gate width are almost identical to that of the wide gate MOSFET.

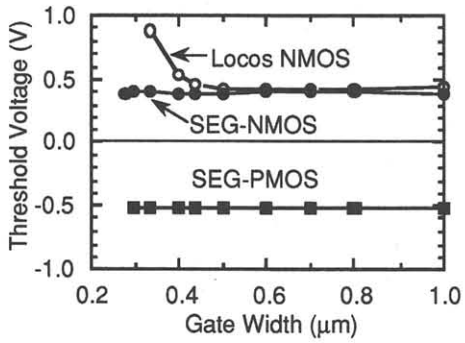

Fig.5 Narrow channel effect of SEG and LOCOS devices.

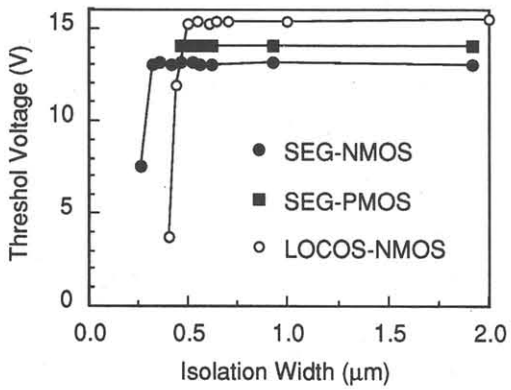

Fig.6 The field threshold voltage as a function of the isolation width for SEG and conventional LOCOS MOSFETs.

Fig.6 reveals threshold voltage of field parasitic transistors as a function of isolation width. The isolation is completed at the isolation width more than 0.3μm. Since the impurity concentration underneath the isolation oxide is $1x10^{17}$ cm^{-3} for N-MOS and $9x10^{16}$ cm^{-3} for P-MOSFET, it seems to be possible to improve isolation characteristics at the isolation width less than 0.3μm by increasing the impurity concentration.

The maximum transconductance Gmmax at the drain voltage at 2.0V was measured at the various gate width. The Gmmax is almost constant at the gate width more than 0.3μm, and the Gmmax is decreased at the gate width of 0.2μm, which means that the difference between the gate width (the measured width of the active region) and effective gate width can be negligible compared with 0.3μm.

In addition, Fig.7 shows the drain voltage - drain current characteristics of ultra short and narrow N-MOSFET which has the gate length of 0.1μm and gate width of 0.3μm. The maximum transconductance Gmmax at the drain voltage of 2.0V is 530mS/mm.

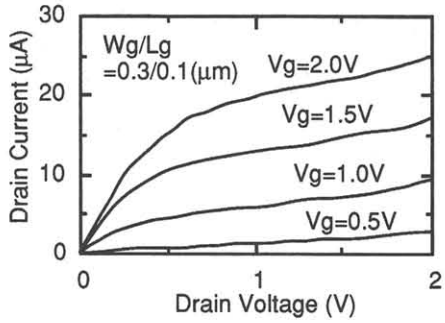

Fig.7 Id-Vd characteristics of ultra short (0.1μm) and narrow (0.3μm) NMOS. Gmmax (sat) is 530ms/mm.

4. CONCLUSIONS

In conclusions, a novel SEG MOSFETs using Ultra High Vacuum CVD has been proposed for sub-quarter micron Si ULSIs. It is found that the junction leakage current and the isolation leakage one are compatible with that of the conventional bulk LOCOS MOSFET. The narrow channel effect was suppressed and the maximum transconductance Gmmax reaches 530mS/mm for ultra short (0.1μm) and narrow (0.3μm) channel N-MOSFET.

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