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Turn-Off Transient Analysis of a DMOS Device Considering Quasi-Saturation

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Abstract

This paper reports the turn-off transient of a DMOS device considering the quasi-saturation behavior. Based on the 2D simulation result, during the input ramp down period of 100ps, the accumulated electrons below the gate oxide are pushed toward the p region below the lateral channel toward the source causing a surge in source current. After the input ramp, these electrons are withdrawn from the drain by the quasi-saturation current.

Summary

In this paper, turn-off transient behavior of a DMOS device is analyzed. As shown in Fig. 1, the DMOS device used in this study has the following characteristics. Under the gate oxide, a lateral channel of $1.3\mu m$ with a peak doping density of $3 \times 10^{17} cm^{-3}$ is formed by double-diffused technology. Below the lateral channel, an n-epi layer of $11\mu m$ with a doping concentration of $1 \times 10^{15} cm^{-3}$ (N_D) is used to sustain a high voltage. An N+ polysilicon gate with an oxide thickness of $500\mathring{A}$ has been used. In order to simplify the analysis, only half of the device is studied. The distance from the right edge of the lateral channel to the right end of the device cross section is $5\mu m$ (L_D). The drain end is connected to $40V$ and the source end is grounded. By imposing an input step from 20V to 0V, turn-off transient analysis of the DMOS device has been obtained.

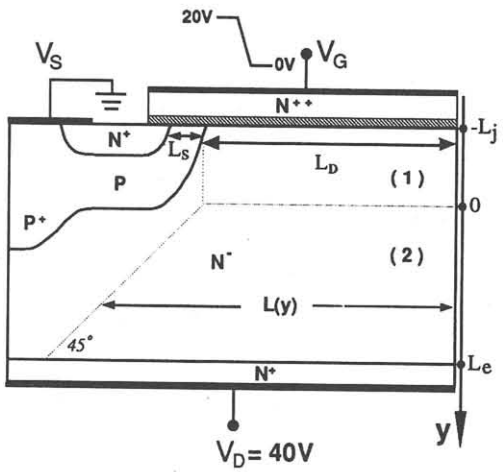

Fig. 1. The DMOS device cross section under study. The substrate doping density is $10^{15} cm^{-3}$. The gate oxide thickness is $500\mathring{A}$. The drain end is connected to 40V and the source is grounded.

Figs. 2(a)&(b) show the drain current and the source current (I_D, I_S) during the turn-off transient of the DMOS device for the input voltage ramps down from $20V$ to $0V$ in 1ns, 500ps, and 100ps. Also shown in the figures are the total electrons flowing out of the drain and the source contacts (Q_D, Q_S) during the turn-off transient. As shown in the figure, as the input ramps down slowly, the surge in the source current looks small. On the other hand, during the ramp down period ($t < t_f$), the drain current tends to be similar regardless of the input fall time. After the input ramp down time ($t > t_f$), the $100ps$ fall time case seems to have a persistent drain current, which indicates charges are still being removed after the input fall time. Among three fall time cases, the $100ps$ fall time case shows the largest change in the source current. It has a huge source current during the ramp down period. As shown in Fig. 2(b), for a large ramp down time (1ns), the electrons in the device tend to be removed from the drain end. On the other hand, for a ramp down time of $100ps$, a large amount of electrons are withdrawn from the

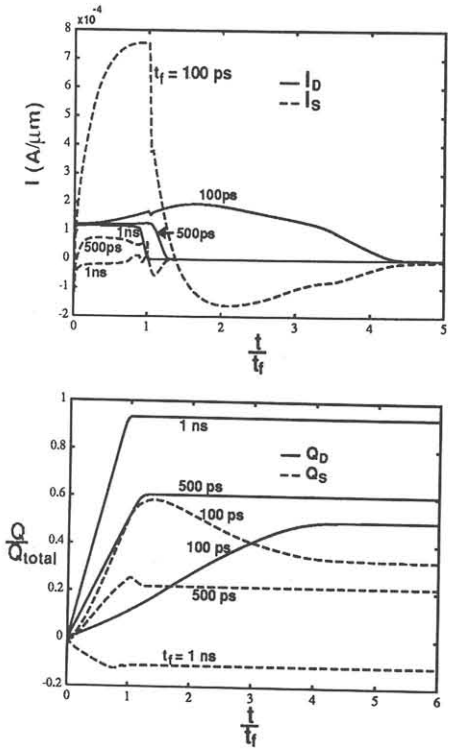

Fig. 2. (a) The drain current and the source current (I_D, I_S) (b) the total electrons flowing out of the drain and the source contacts (Q_D, Q_S) during the turn-off transient of the DMOS device for the input voltage ramps down from $20V$ to $0V$ in 1ns, 500ps, and 100ps. The total electrons have been normalized by the initial total electrons in the n-epi region and the lateral channel region (Q_{total}). The time has been normalized by the fall time.

source end. Different from the other two cases, with an input ramp down time of $100ps$, during the initial period, the total electrons removed from the source end are even more than those from the drain end. With a quick fall time, what happens in the DMOS device seems to be interesting.

Figs. 3 show (a) the 2D current flow lines (b) the electron density in the DMOS device during the turn-off transient of the DMOS device with an input fall time of $100ps$. As shown in the figure, at 50ps, most of the current flows are from the source end via below the lateral channel region instead of via the lateral channel. At $50ps$, in addition to the accumulated electrons at the silicon surface, electrons also gathers in the p- region below the lateral channel. At the end of the input ramp, more current flow lines via the p- region below the lateral channel and more electrons in the p-region can be identified. This implies that the sudden down-fall of the input voltage makes the junction between the p- region and the n-epi substrate

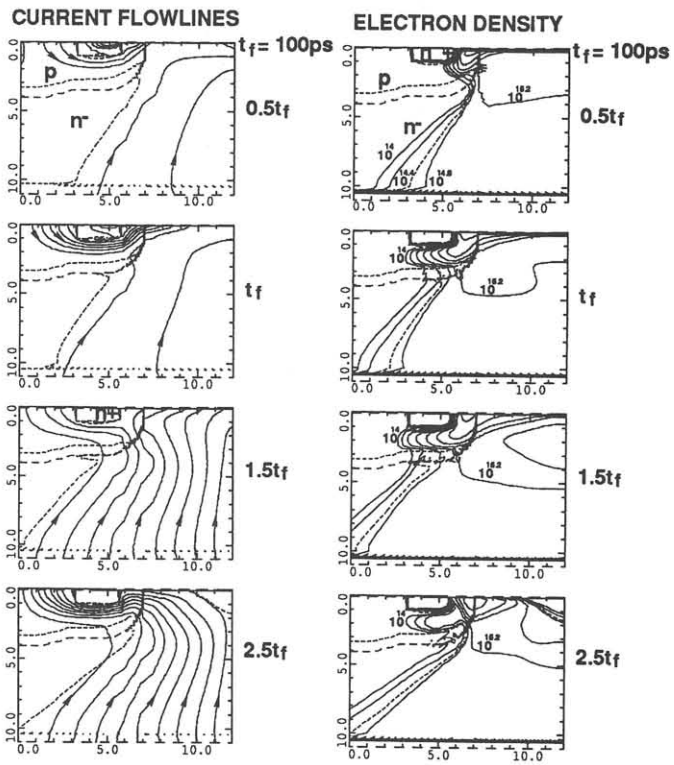

Fig. 3. (a) The 2D current flow lines (b) the electron density in the DMOS device during the turn-off transient of the DMOS device with an input fall time of $100ps$. Each flow line represents one tenth of the total current.

forward biased since the potential at the surface electron accumulation region becomes much more negative than the potential in the p- region. As a result, the accumulated electrons at the silicon surface are forced to be pulled out of the source contact via the p- region. At this time, a smaller amount of current flows in the n-epi region to the drain contact. After the input ramp-down period at 150ps, the current in the p- region reverses its direction. Instead of flowing from the source terminal, the current in the p- region is flowing from the drain current. This indicates, the electrons are pulled toward the n- epi substrate direction. At 250ps, the current in the n-epi region seems to be persistent and the electrons in the p- region are decreasing.

The persistent drain current during the most of the transient period for the 100ps fall time case can be understood by studying the electron density and the electric field in the vertical direction at the right end of the cross section of the DMOS device during the turn-off transient as shown in Figs.4. As shown in the figure, during the overall transient period, the electron density distribution in the vertical direction in the n-epi substrate

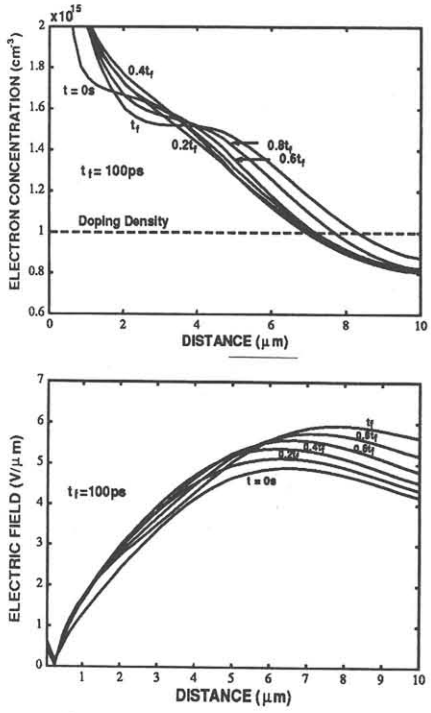

Fig. 4. (a) The electron density and (b) the electric field in the vertical direction at the right end of the cross section of the DMOS device during the turn-off transient with an input fall time of $100ps$.

tends to stay rather fixed – in the quasi-saturation situation with its conduction area reaches its maximum [1]. Throughout the turn-off transient, the electric field in the vertical direction is consistently over the critical electric field ($E_c = 0.8V/\mu m$). Therefore, the electrons are travelling at a saturated velocity toward the drain terminal. Considering the trapezoidal-shape conduction area in the substrate region, the electron current in the vertical n-epi substrate region is constant at each location. This means that the n-epi region, the electron density profile stays almost unchanged as in the dc quasi-saturation situation during the turn-off transient. During the turn-off transient, the accumulated electrons at the silicon surface need to be removed. However, the current via the n-epi region stays steady makes the charge removal via the n-epi region rather difficult – quasi-saturation affects the charge removal process. Therefore, initially, the accumulated electrons are removed from the source end via the p-region.

Fig. 5 shows the equivalent circuit of the DMOS device during the turn-off transient for a fall time of $100ps$. During the input ramp down period ($t < t_f$), the equivalent circuit is composed of the "channel-to-gate capacitance" (C_{cg}) between the gate and the transition location (V_{ch}), the quasi-

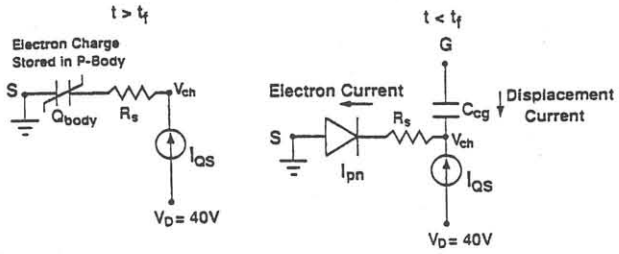

Fig. 5. Equivalent circuits of the DMOS device during the turn-off transient. (a) $t < t_f$. (b)$t > t_f$.

saturation current (I_{QS}), and the pn junction between V_{ch} and the p- region with the substrate resistance R_s. As input ramps down quickly in $100ps$, the accumulated electrons below the gate oxide near V_{ch} are being pushed toward the p region due to the forward bias of the pn junction between the p region and the n-epi region. As the gate voltage is lowered suddenly, the displacement current over C_{cg} lowers the potential in the electron accumulation region below the gate oxide. As a result, the pn junction between the electron accumulation region at the silicon surface and the p-region is forward biased. The accumulated electrons at the silicon surface are being pulled toward the p- region. Therefore, a surge in the source current can be seen as shown in Fig. 2. In addition, a lot of electrons are being stored in the p- region. During the input ramp down period, the quasi-saturation current (I_{QS}) remains the same due to the fact that the conduction area in the substrate epi-region already reaches its maximum trapezoidal-shape area [1]. In other words, instead of being removed from the drain end, the accumulated electrons under the gate oxide are forced to be removed via the p- region to the source contact although the drain potential is much higher. After the input ramp down period ($t > t_f$), the effect of the displacement current is not important any more. During this time, the equivalent circuit is composed of the quasi-saturation current (I_{QS}) and the nonlinear capacitance accounting for the stored electrons in the p- region (Q_{body}) as shown in Fig. 5(b). As $t > t_f$, the stored electrons in the p-region are being removed from the drain contact by the quasi-saturation current.

References

[1] C. M. Liu, K. H. Lou and J. B. Kuo, *IEEE TED*, Sept. 1993