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Study of an Epitaxial Ferroelectric / Semiconductor / Insulator Structure Using Perovskite Oxides for Application to the Field Effect Transistor

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Using its metal- insulator (M-I) transition and excellent structural compatibility to ferroelectric perovskites, perovskites oxide having 3d metal element is used as the semiconductor in a metal/ferroelectric/semiconductor field effect transistor for the first time. The cuprate oxides having low carrier density is found to be an excellent semiconductor in this structure and basic properties of epitaxially grown ferroelectric / semiconductor/insulator hetero-structure are presented. The feasibility of this memory for commercialization is discussed and possibility for high density integration is suggested.

Solid-state non-volatile memories have recently received considerable interest. Among such memories, the fast speed and the high density are expected for the ferroelectric random access memory (FRAM)[1] and for the metal/ ferroelectric /semiconductor field effect transistor (MFS-FET) which was proposed in 1957[2-5] and was demonstrated in 1963[6]. The field effect transistors (FET) were intensively studied[7-13], and the MFS-FET, which uses ferroelectric as a gate insulator instead of dielectric in a FET, was a natural byproduct of such researches.

There have been numerous attempts to realize the MFS-FET [14-19]. In all these trials Si was used as a semiconductor except a use of CdS in ref.[2]. On the other hand, various ferroelectric materials including non-oxides[16,19] were tested. However, all reported MFS-FETs without intermediate layer showed an instability i.e. a loss of memory. Moreover a theoretical predictions were made showing that the MFS-FET could not be realized [20]. The memory retention was markedly improved by inserting intermediate layer such as SiOx and SiNx. But this made the MFS-FET very slow[15] contrary to the fast switching capability of the ferroelectric. Hence, recent efforts to realize ferroelectric non-volatile memories are mostly directed to the FRAM.

We propose a novel MFS-FET structure which can overcome these problems. Considering the history, we made a new approach described below. First of all we conclude that it is extremely difficult to form oxides on non-oxides at an elevated temperature without forming an extra-oxide layer, i.e., a reaction layer, based on our previous study [21]. This means that the use of an intermediate layer is inevitable to grow a ferroelectric perovskite on a non-oxide. Generally, O,F, Cl and Br contained in the ferroelectric film would easily react with the semiconducting layer unless the semiconducting layer is a compound of such element «P1». Especially, the semiconductor layer should be of oxide when the ferroelectric layer is chosen to be of perovskite oxide. Next, we tentatively postulate that the memory should be retained, if the interface between the ferroelectric and the semiconductor is free of traps which would be excessively generated by structural disorder and defects. In Si-FET, combination of Si and its dielectric compounds are used to solve this problem, and modulation of composition is used in III-V system. In accordance with such conventional approaches, we propose the "*all epitaxial ferroelectric/ semiconductor hetero-structure*" «P2» for a MFS-FET which was not pursued by far, while similar structures are already proposed for the capacitor structure[22]. Figure 1 compares the several approaches to MFS-FET including present one.

The ferroelectric perovskite/semiconductive perovskite system is one of the rare structures which fulfill the requirements «P1» & «P2». It would be fair to refer to the superconducting FETs employing dielectric perovskite/ perovskite superconductor structure[23-25]. However, any device which uses superconductivity would be difficult to find a large market, due to a low-temperature operation. Furthermore the modulation of the conductivity in these FETs is intrinsically small at room temperature due to a large carrier concentration. Because of a revolutionary increase of the superconducting transition temperature, most researches on cuprate (or high-Tc) superconductors seem to be confined in the regime of superconductivity and thus to be missing new possibilities of these compounds. The idea to use high-Tc cuprates just as a metal electrode without superconductivity referred above[22] as well as the present proposal is an innovation which jumped out of the obsession of superconductivity.

Various investigations have revealed that the electrical properties in the superconducting state of the high-Tc cuprates are relatively similar to the conventional superconductors while those in non-superconducting state are abnormal [26-29]. This is natural from view point of a generalized BCS

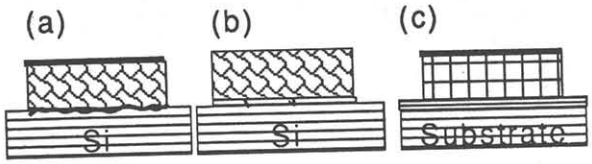

Fig.1 MFS-FET structures. ferroelectric/Si (a), ferroelectric/SiOx(b), present structure(c).

theory[30], because the the most phenomena in super-conducting state are the thermodynamic and renormalized phenomena which are independent of a specific origin. One of the unusual properties of the high-Tc cuprates is the drastic change of electronic state from the insulator(I)(e.g. La_2CuO_4) to the metal(M) (e.g. $La_{1.85}Sr_{0.15}CuO_4$) by change of the doping density [31]. Corresponding this change, free-electron like state i.e. Drude like electronic state evolves rapidly as doped [26,29] (Fig.2). Similar phenomena are also found in many 3d metal oxides including LMO_3 type perovskites (L= rare earth element, M=3d transition metal element) exhibiting a M-I transition (e.g. $LaMO_3$(=I), $La_{0.7}Sr_{0.3}MO_3$(=M))[29]. We have assumed that we could modulate the conductivity in these semiconducting phases, which are not described by conventional band models[31], by the field effect, and moreover that a drastic change in the conductivity could be potentially attained by *inducing "construction and destruction of electronic correlation" by the field effect.*

The insulating nature in such oxides results from the strong electronic correlation such as the magnetic order. In insulating or semiconducting phases (e.g. La_2CuO_4, $LaMO_3$) of such perovskites, conductivity was observed to change by substituting a part of metal element by other metal elements. However, no field effect, by which the conductivity should be increased at a gate bias and be decreased at the opposite gate bias, has been reported in these semiconductive phases[32] except the observation at 5K in a YBaxCuyOz film having a unidentified structure [33]. Judging from the conductivity at 5K, the film in ref.[33] seems to be metallic at room temperature. On the other hand, the electronic correlation is known to reduce in the doped i.e. the metallic phases[26], and weak field effects are reported[23-25]. We have observed a field effect at R.T. in semiconducting

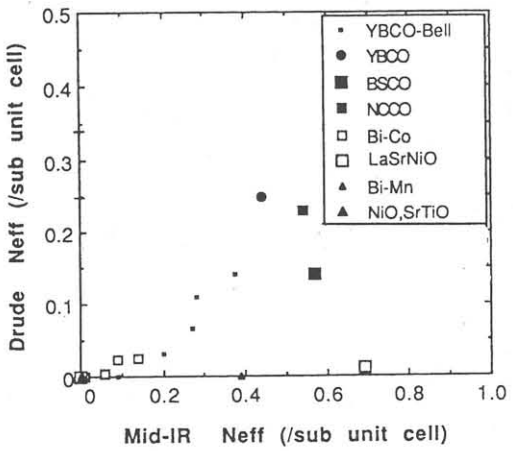

Fig.2 Evolution of free electron(Drude)state vs. the state in the charge transfer gap(Mid-IR) by chemical substitution[29].

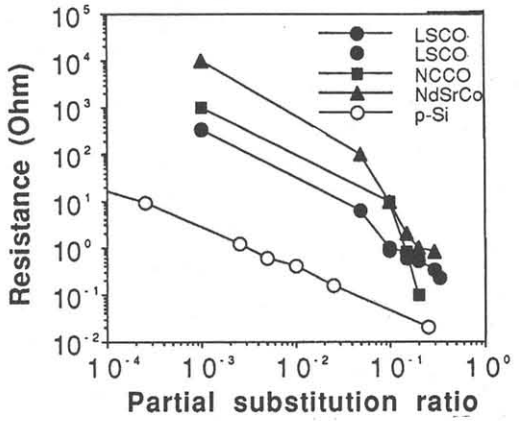

Fig.3 Resistivity vs. fractional substitution(x) at 300K in $La_{2-x}Sr_xCuO_4$ (film & single crystal [26]), $Nd_{2-x}Ce_xCuO_4$ (film), $Nd_{1-x}Sr_xCoO_3$ (poly-crystal), Si:Bx[35].

perovskite films for the first time to our knowledge [34]. The merit of the M-I transition is that this occurs at relatively high carrier density as shown in Fig.3, which can suppress instability due to the depolarization field[20]. From the above discussions, it is expected that the proposed "all epitaxial ferroelectric/ semiconductor hetero-structure" can have a well defined interface and a capability of the memory retention by the ferroelectric polarization.

To model the basic operation mechanism of MFS-FET, we have modified a conventional model for the FET [35], by describing operation in terms of charge density and the polarization instead of the field intensity and the voltages [36]. According to this model, carrier density times thickness under the gate should be about the same as the remnant polarization. This requires ferroelectric perovskite/ ultra-thin semiconductive perovskite / insulating substrate structure,

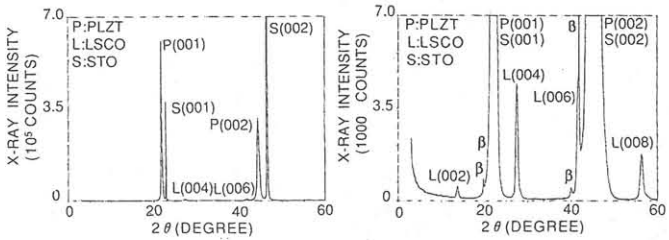

Fig.4 θ/2θ x-ray diffraction pattern (a) and its blow-up (b)

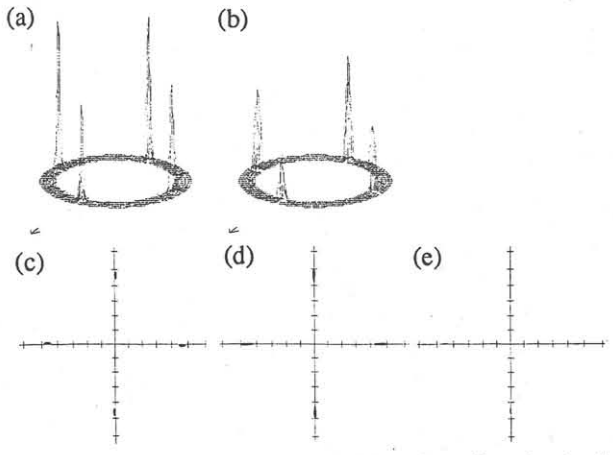

Fig.5 Pole figures of ferroelectric(a) and semiconductive(b) layers and their projections((a)→(c),(b)→(d),substrate(e)).

since the defect density in perovskite semiconductor is not as low as in Si. Results of the basic studies on one of these ferroelectric perovskite/ semiconductive perovskite /insulating substrate hetero-structures are discussed below.

Figures 4 and 5 show that the high degree of crystallographic perfection is achieved in a proposed hetero-structure. Three dimensional alignment of each layer is evident in the θ/2θ scan x-ray diffraction pattern and the pole figures of $Pb_{0.9}La_{0.1}Ti_{0.8}Zr_{0.2}O_3$(2000A) / $La_{1.99}Sr_{0.01}CuO_4$ (150A)/ $SrTiO_3$ substrate. Hereafter we denote $La_{2-x}Sr_xCuO_4$ as LSCO(x). No secondary phase was observed even in the blow up of Fig.4a (Fig.4b). This was evidenced by depth profiles of the Auger electron spectroscopy and by the absence of secondary phases in annealed samples [37].

The ferroelectric properties of the hetero-structures deposited with gold electrodes are were measured by using a Sawyer-Tower circuit. Unlike the ferroelectric on a metallic electrode, the hysteresis was rounded due to the apparent tanδ caused by a high resistance of the semiconducting electrode. The measured dielectric constant decreased as the resistance of LSCO layer increased. Nevertheless, we have not observed the difference between dielectric constants of the samples having heavily doped thin LSCO(x=0.05~0.1) layers and those having lightly doped thick LSCO(x=0.0~ 0.01) layers. Additionally, the dielectric constants of the samples having high resistance LSCO layers approached to those having low resistance LSCO layers as the frequency of the applied voltage decreased(~10Hz)[R]. The behaviors of dielectric constant are simply understood by a RC time constant. We suspect that the suggestion of instability in ferroelectric/semiconductor structure[20] might have missed this cause. Figure 6 shows ferroelectric hysteresis curve observed in the hetero-structure having LSCO(x=0.01), where the resistance of the LSCO layer (the RC constant effect) is compensated by a 11Ω resistor serial to a reference capacitor. The remnant polarization was $\pm 8\mu C/cm^2$ which should be sufficient to modulated the conductivity of a LSCO layer by a few tens percent. The shape of the obtained hysteresis suggest that the hetero-structure did not have the instability[20] at least for LSCO(x=0.01). These results encourage the present approach to a MFS-FET, and measurements of the memory effect are currently in progress.

Finally we address potentialities of the present MFS-FET. The expected advantages of the MFS-FET are the aerial bit density, the speed and the reliability. To be competitive with other non-volatile memories, the bit density should not be much less than that of the rigid disks. This requires the size of the MFS-FET to be below 500nmx500nm and thus the length of the gate to be below 200nm. In case of ferroelectric/Si structure, this requires a very thin channel which is not damaged by the reaction with ferroelectric. This may be a severe constraint in this structure. In the present MFS-FET

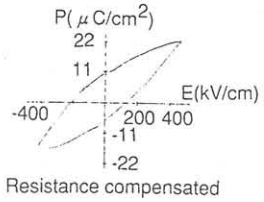

Fig.6 D-E hysteresis of hetero-structure(1kHz,dark).

which uses ultra-thin semiconductor layer, the short channel effect[31] is well suppressed, enabling a higher bit density. The metal/ferroelectric/insulator/Si(MFIS) [38] and the metal/ ferroelectric/metal/insulator/Si(MFMIS)[39] structures may not be also suitable to a dense integration due to the structural complexity and the excessive height of the gate area. The use of special electrode materials[40] in the latter structure to reduce the fatigue makes the gate even higher. The fatigue of ferroelectric films is reported to be also solved by use of epitaxial structure[41], which is already incorporated in the present hetero-structures. Moreover, the memory function will be lost in these structures, if the charges are transported through the insulating buffer layers. This problem would not exist in the present MFS-FET.

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