Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 787-789

InAs Field-Effect Transistors with Platinum Schottky Gate

Kanji Yoh and Hayato Takeuchi
Research Center for Interface Quntum Electronics, Hokkaido University
N13 W8, Kita-ku, Sapporo 060 Japan

Satoshi Izumiya and Masataka Inoue
Department of Electrical Engineering, Osaka Institute of Technology
5-16-1 Omiya, Asahi-ku, Osaka 535 Japan

We have successfully demonstrated that the deposition and subsequent alloying of platinum gate would dramatically improve the current-voltage characteristics of InAs heterojunction FETs based on antimonides. The removal of the surface oxide / defects and in-situ formation of clean Schottky interface by the surface reaction presumably caused the dramatic improvements. The technique may be applicable to other hetrojunction FETs, especially when high aluminum compound ratio is involved.

1.Introduction

High performance InAs heterojunction field-effect transistors based on antimonides have been shown to have higher potential in achieving high transconductance[1-2] compared with conventional HEMTs based upon GaAs or InGaAs-channel FETs. However, it has been known that it is difficult to achieve decent drain-current modulation characteristics by the gate voltage application[3]. It was suspected that the AlGaSb or AlSb barrier material easily gets oxidized because of its high aluminum contents and hence degraded gate voltage swing. One of the solutions would be to make use of the clean Schottky junction formation by the surface reaction of the gate material and the semiconductor. Platinum gate has been known to react with GaAs surface forming controllable clean Schottky junction, i.e., $PtAs_2$/GaAs[4-5]. This technique was mainly applied to GaAs MESFETs to control the threshould voltage[6]. We have applied this technique on InAs/(AlGa)Sb heterojunction transistors and obtained dramatic effect in achieving high yield of decent FET operation.

2.Experimental

The heterostructure of the devices consists of 2000 Å of GaAs buffer layer grown on undoped GaAs substrates, 1μm of AlSb buffer layer, 2000Å of AlGaSb layer, 150 Å of InAs channel layer, 150 Å of AlGaSb top barrier layer, and 100 Å of GaSb cap layer. A fairly standard fabrication procedure commonly used in GaAs device fabrication was employed: the device isolation was done by phosphoric-acid-based etchant, Au/Ge/Ni/Au was used as ohmic metal. The deposition

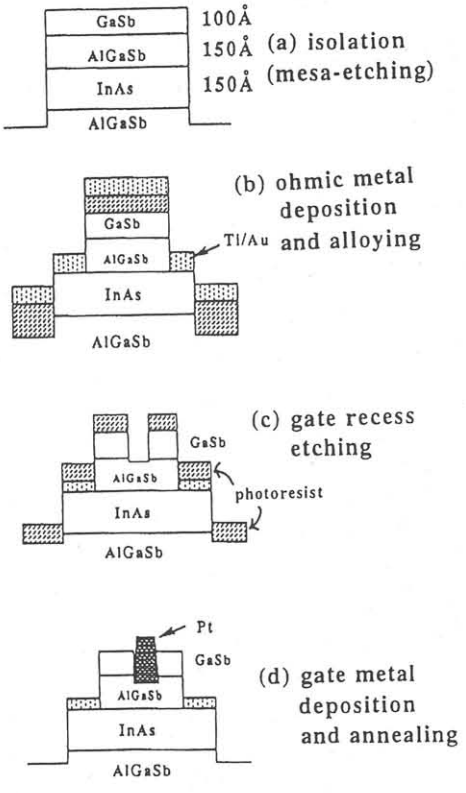

Fig.1. Process flow of InAs heterojunction FET with platinum gate ("Process A")

and alloying procedure were conducted in two ways. First procedure was to deposit platinum metal after ohmic metal deposition and anneal as for the normal HEMT or MESFET fabrication. Let it be called "process A". The process flow is shown in Fig.1. The advantage of this process is that the I-V characteristics dependence on the annealing condition of the very same device can be traced. The disadvantage of this process is that the quality of the ohmic contact may degrade during the annealing procedure, which in turn affect the transitor characteristics. Second procedure was to deposit and anneal platinum metal prier to the non-alloyed ohmic metal deposition so that ohmic contact does not degrade during the gate metal anneal. Let it be called "process B". The process flow is shown in Fig.2. The advantage of this process is that the ohmic contact does not degrade with gate metal annealing procedure. In both cases, three annealing conditions were examined: non-anneal, 2 minutes and 6minutes anneal at 360°C.

3.Results and Discussions

The current voltage characteristics of an InAs FET fabricated by "process A" is shown in Fig.3. Improvements of current modulation was clearly observed in the current voltage characteristics of an InAs FET fabricated by "process A". However, because of the disadvantage of the present procedure, i.e. ohmic contact degradation, improvements of the I-V characteristics was not as dramatic as expected. Although the current voltage characteristics show imperfect pinch-off of the channel, threshould voltage shift due to the alloying process is appreciably large and it moves toward positive direction. The amount of the threshold voltage shift between 2 minutes anneal and 6 minutes anneal is approximately 0.5 V.

The current voltage characteristics of InAs FETs fabricated by "process B" is shown in Fig.4. The improvements of the current voltage characteristics by the present procedure were dramatic. The transconductance of the hardly operating device has been improved to show 80mS/mm. Considering the average crystal quality of the present device, the improved maximum transconductance is good enough to verify the effectiveness of the platinum gate approach

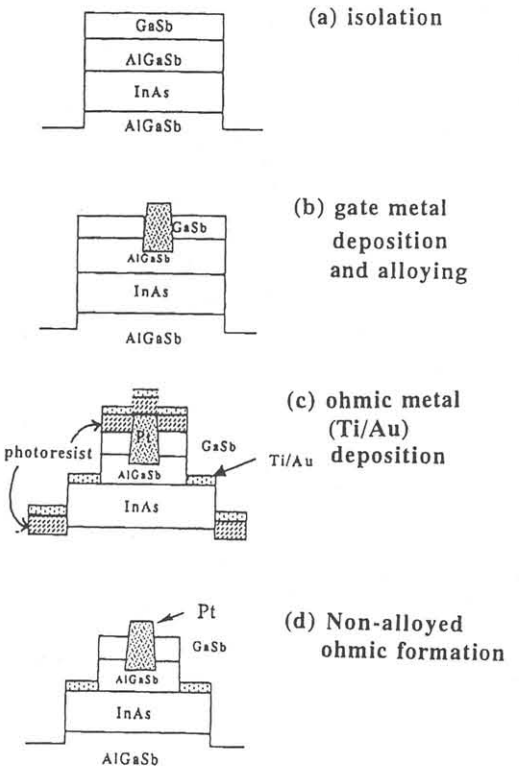

Fig. 2. Process flow of InAs heterojunction FET with platinum gate ("Process B")

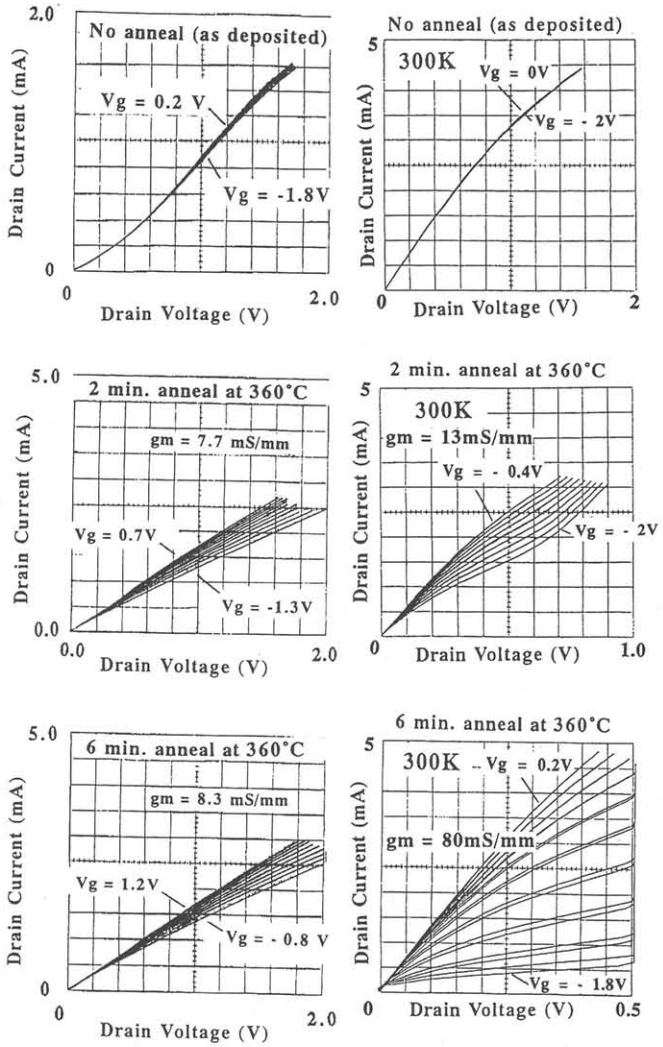

Fig.3. Current voltage characteristics of an InAs heterojunction FET fabricated by "Process A".

Fig.4. Current voltage characteristics of InAs heterojunction FET fabricated by "Process B".

to improve InAs FETs based on antimonides. Similar approach may also be useful for the heterosjunction FETs with barrier materials which contain high aluminum compound ratio. The physical model of the improvements is schematically illustrated in Fig. 5. Initially, the FETs which show poor current modulation by the gate voltage scan are presumably caused by the voltage drop at the interface layer between the Schottky gate and the GaSb cap layer. The surface reaction of the platinum with the underlying semiconductor creates conductive alloy layer between the platinum gate and the semiconductor. The surface semiconductor reacts with the platinum to change into some conductive alloy ($PtAs_2$ when this was applied to GaAs[5-6]), pushing the Schottky interface front towards the channel while maintaining the clean interface during the surface reaction. The present model can explain the threshould voltage shift observed in the devices of process A and the dramatic improvements of the current modulation as seen in Fig.4 (process B) by the removal of interface layer during the surface reaction.

The statistics of the device characteristics in various process conditions are listed in Table I. The samples whose yield was initially only 9% have been improved to give 37% by two minutes alloying at 360°C, and then reached the yield of up to 57% by the 6 minutes alloying at 360°C. Severe gate leakage current of the samples which underwent the 4 minutes alloy at 410°C suggests that the platinum alloy have reached at the InAs channel by the surface reaction.

4.Conclusions

We have successfully demonstrated that the deposition and subsequent alloying of platinum gate would dramtically improve the current-voltage characteristics of InAs heterojunction FETs based on antimonides.

Acknowledgements

The authors are grateful to H.Kawahara for the technical assistance in the device fabrication and measurement. This work was partially supported by Grant-in-Aid for Scientific Research from The Ministry of Education, Science and Culture.

References

[1] G.Tuttle, H.Kroemer and J.H.English: J. Appl. Phys. 65, 5239 (1989).

[2] K.Yoh, T.Moriuchi and M.Inoue, IEEE Electron.Device Lett., 11, p.526 (1990)

[3] Private communication with M.Mizuta of NEC Corporation and with H.Kroemer of UCSB.

[4] D.J.Coleman et al, Appl.Phys.Lett., Vol.24, 365 (1974)

[5]N.Toyoda et al, Proceedings of the International Symposium on the GaAs and Related Compounds, vol.63, p521 (1981)

[6] N.Toyoda et al, Jap.J.Appl.Phys., vol.22, Suppl.22-1, 345 (1983)

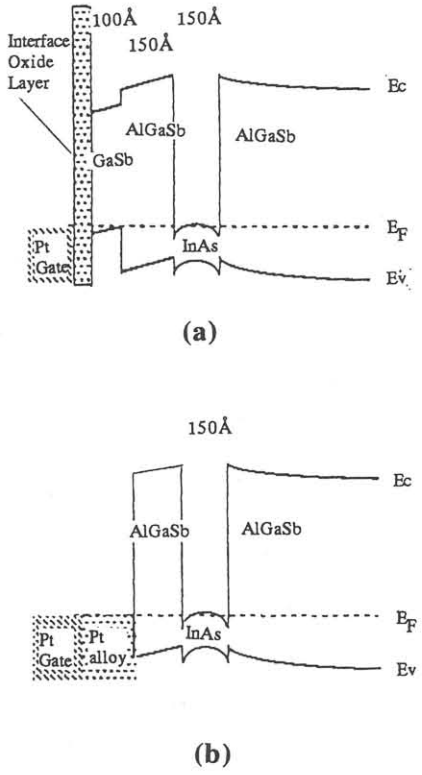

Fig. 5. Schematic energyband diagram of a platinum gated InAs/AlGaSb HFET (a) before and (b) after Shottky gate alloy.

Table I. Statistics of working samples with various alloying conditions.

Alloying Condition	Number of samples with decent current modulation	Number of samples with poor current modulation	Number of samples which suffer from severe gate leakage
No anneal	1	1	9
2 min. at 360°C	7	8	4
6 min. at 360°C	29	19	4
4 min. at 410°C	0	12	29