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Hardware-Oriented Learning Algorithm Implemented on Silicon Using Neuron MOS Technology

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We have developed a basic hardware organization for neural networks using "brain-cell-like" transistor called *Neuron MOSFET* (*νMOS*) as a key element and a newly developed EEPROM synapse cells. In order to provide a self-learning capability to the neural network hardware, a new hardware-oriented learning algorithm called *Hardware Backpropagation* (*HBP*) has been developed by simplifying the original Backpropagation algorithm aiming at facilitating its on-chip circuitry implementation. The self-learning performance of νMOS neural networks has been verified by a learning simulator which has been developed for optimizing the pertinent circuit parameters.

INTRODUCTION

Neural networks are now focused as a new paradigm of information processing because of its self-adapting capability in solving problems. In order to accommodate a neural network hardware to existing learning algorithms, the chip needs an off-chip supervisor computer, or otherwise consumes a large chip area for learning control circuitry. For the purpose of high-density integration of a neural chip having an on-chip self-learning capability, it is critically important to develop a new learning algorithm specifically designed to facilitate on-chip circuitry implementation. For this purpose, we have developed a new hardware-oriented learning algorithm called *Hardware Backpropagation* (*HBP*), which is a simplified and modified version of the original Backpropagation (BP) algorithm [1]. One of the most important features in HBP is the introduction of the concept of "Learning Enhancement": the learning of a network (weight modification) is forced to continue even if it gives a right answer until the NET (weighted sum of inputs for a neuron) is well shifted away from the threshold point. This is important to guarantee a long-term stability of the learned state of a neural network. The purpose of this paper is to present the HBP algorithm and its circuit implementation using νMOS technology.

NEURON CELL AND SYNAPSE CELL

A νMOS has a floating gate and multiple input gates which are capacitively coupled to the floating gate [2]. The linear sum operation of all input signals is carried out via capacitive coupling at the floating gate, and on and off states of the transistor is controlled by the potential of the floating gate. A neuron cell configuration composed of a complementary νMOS inverter and an ordinary inverter, is shown in Fig. 1. The neuron fires when the potential of the floating gate (dendrite) exceeds the inverting threshold of the νMOS inverter.

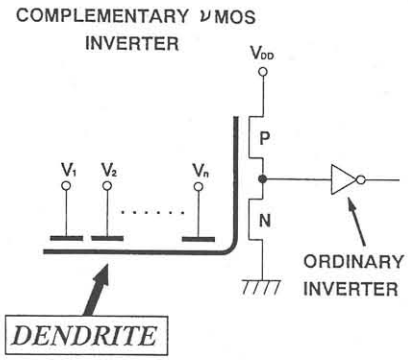

Fig. 1. Circuit diagram of νMOS neuron cell.

The synapse circuit shown in Fig. 2 is provided to each synaptic connection to make the connection strength adjustable [3,4]. The synapse cell stores analog weight data as charges on the floating gate and transfers the weight value to the input gate of a neuron nondestructively by the action of N- and P-νMOS source followers. The source followers are merged into CMOS inverters to cut off the DC current paths, thus realizing low-power feature. The change in the synaptic weight can be accomplished by selecting the high-voltage program lines, V_X and V_Y, in a similar manner to the programming of dual-control-gate EEPROM cell [5]. Namely, only at cells where both V_X and V_Y are high, the weight modification (charge

injection) occurs. All synapse output voltages are transferred to the neuron floating gate (dendrite) via identical coupling capacitances.

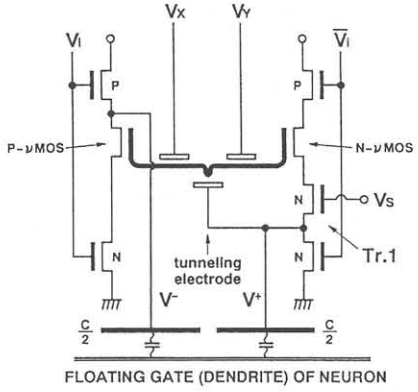

Fig. 2. Circuit diagram of seven transistor synapse cell.

HARDWARE LEARNING

Hardware Backpropagation (HBP) is a simplified and modified version of the original Backpropagation (BP) algorithm [1] as illustrated in Fig. 3. The sigmoidal function are replaced by a step function so that it matches to the output characteristics of the νMOS neuron cell. Its derivative in original BP are replaced by a window function, which are most easily realized by νMOS circuitry. Here NET=−1, 0 or 1 on the abscissa corresponds to the neuron floating-gate potential of 0, $V_{DD}/2$ or V_{DD} on the hardware. δ represents the "error parameter" to backpropagate for weight modification. α specifies the marginal region within which the weight modification is continued for "learning enhancement." This is important to guarantee a long-term stability of the learned state of the chip against disturbances such as the charge loss in EEPROM synapse memories or the noise in threshold operation of neuron cells.

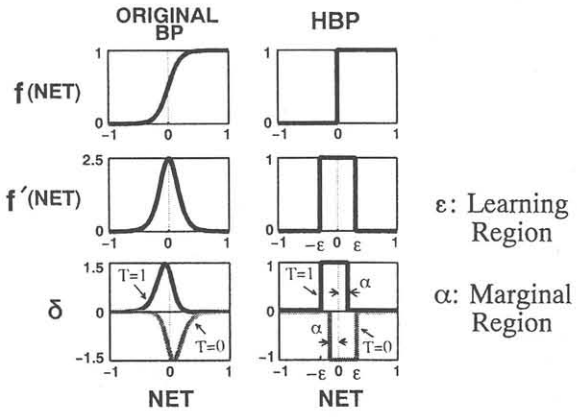

Fig. 3. Comparisons of original BP and HBP.

A photomicrograph of an experimental νMOS neural network chip is shown in Fig. 4, where the HBP algorithm is implemented in the learning controllers using νMOS circuit technology. The circuit diagram of the learning controller for output neurons is given in Fig. 5. The HBP-parameter generator is utilized to generate the window function in Fig. 3 where the parameter ε is determined by signals V_H and V_L. Similar circuits are also used to define marginal regions (α). The measured output characteristics of the circuit is shown in Fig. 6.

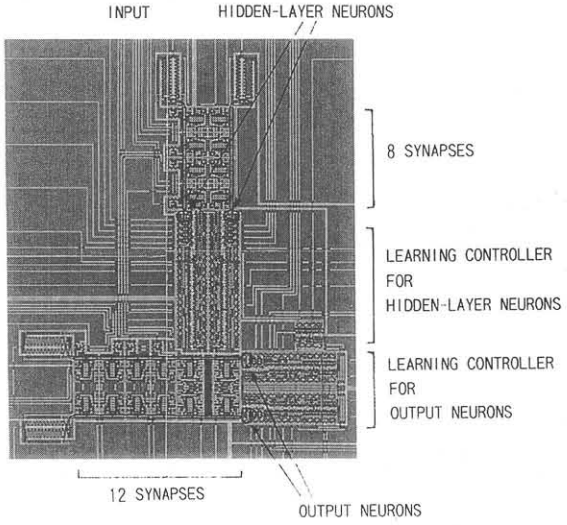

Fig. 4. Experimental νMOS neural network having on-chip learning circuitry, including three input units, two hidden-layer neurons, two output neurons and 20 synapses.

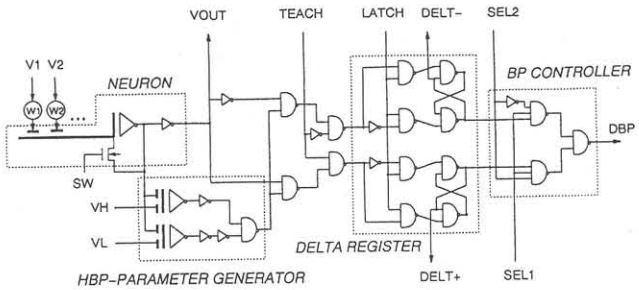

Fig. 5. Circuit diagram of the learning controller for output neurons.

OPTIMIZATION OF HBP PARAMETERS

The optimization of the parameters α and ε was carried out by computer simulation employing three-input XOR learning as a test problem. Learning was performed for 50 different random weight patterns at the initial stage and the presentation was repeated up to 40,000 times. In Figs. 7, 8, and 9, the convergence probability for 50 initial conditions is shown as a function of the learning rate.

Fig. 7 demonstrates the optimization of α for hidden layer neurons. In the marginal region specified

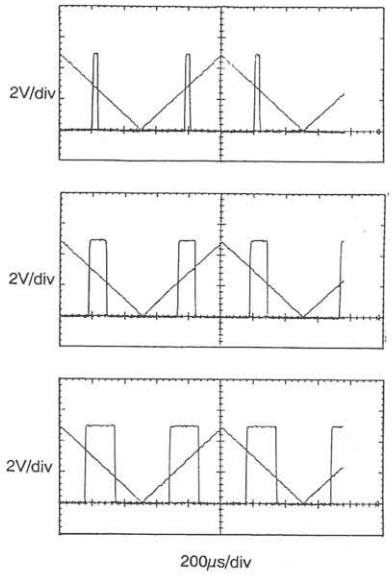

Fig. 6. Measured output characteristics of νMOS window-function generator.

by α, the network is forced to continue learning even after it correctly learns the problem. Therefore the larger the α value, the performance would be expected to degrade. However, it is quite interesting to note that the performance is enhanced with the introduction of α. Such forced learning would help the network to escape from local minima. For this reason α for hidden is set at 0.05.

Further enhancement in the learning performance was carried out by optimizing the window function (ε) as shown in Fig. 8. The largest performance is obtained for stair-case variation of ε, which is very easily performed on hardware by changing V_H and V_L as shown in Fig. 6. The comparison of the learning performance for HBP and BP [6] is given in Fig. 9, demonstrating superior performances of HBP over original BP.

The ability to solve new problems not shown during the learning phase (generalization capability) can not been verified by such a simple problem as XOR learning. The generalization capability of νMOS neural network has been verified for mirror symmetry problem learning and is described in Ref. [7].

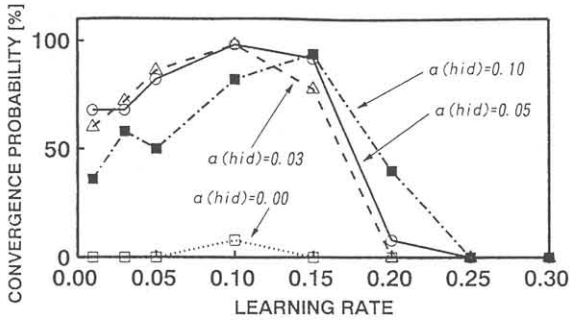

Fig. 7. Performance of three-input XOR learning for various values of marginal region width α for hidden, where α for output is set at 0.03.

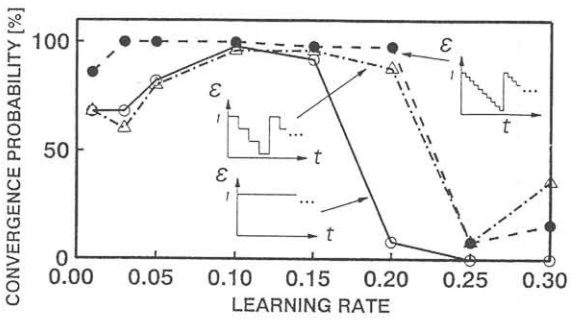

Fig. 8. Learning performance enhancement by stair-case variations in the learning region width ε. The stair-case steps are illustrated in the figure.

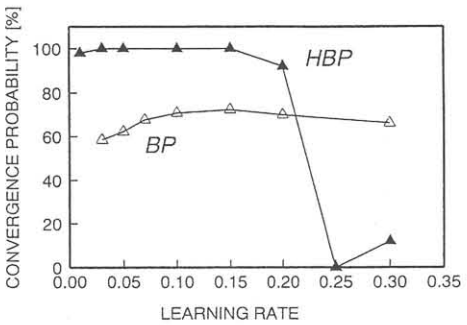

Fig.9. Learning performance comparison between original BP and HBP. Data of BP were taken from Ref. [6].

CONCLUSION

A new hardware-oriented learning algorithm called Hardware Backpropagation (HBP) has been developed for νMOS neural network. By optimizing the pertinent parameters for circuit design using learning simulator, HBP has shown superior learning performance to original BP. We have introduced a new concept of "learning enhancement" for the first time to guarantee the long-term stability of the learned state of a chip, which has also drastically enhanced the learning performance.

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