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Study of Single Layer Thermal Oxide as Inter-Poly Dielectric for Next Generation Flash Memory

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We discuss about the possibility of using a single layer thermal oxide film as the inter-poly Dielectrics(IPD) replacing the ONO film for flash memory. Using an ultra-thin floating gate electrode which is re-crystallized from an amorphous Si, the programming and the disturb characteristics were improved drastically. This study suggests that some applications of the structure of the thermal oxide film/the ultra-thin floating gate electrode for flash memory are possible although a further improvement of the oxide quality is preferable.

1. INTRODUCTION

Scaling of the inter-poly dielectrics (IPD) is one of the most critical issues for the next generation flash memories such as 256Mb and beyond. Thinner inter-poly dielectrics as well as thinner tunnel oxide is key to achieve small cell size and low voltage operation. The ONO films with effective thickness of about 20nm are currently used as IPD. The formation of the ONO films with effective thickness thinner than 10nm are very difficult because the precise control of thickness and quality of each films as thin as a few nm should be required. [1] [2]

In this study we discuss about the possibility of using a single layer thermal oxide film as IPD. As we reported previously [3], an ultra-thin poly Si floating gate electrode which is re-crystallized from an amorphous Si film has some advantages in reducing cell size and realizing a very smooth poly Si surface. We indicate the possibility of using a single layer thermal oxide film as IPD by means of an ultra-thin floating gate electrode structure.

2. SAMPLE PREPARATION

Three different cell transistors shown in Table 1 were fabricated to investigate their cell characteristics. All of them has a stacked gate structure. The ultra-thin floating gate electrode was formed by the deposition of an amorphous Si film with thickness of 150Å and the annealing at 600°C to re-crystallize it, and undergoes no doping steps. A single layer thermal oxide film and an ONO film with a structure of HTO/SiN/Thermal Oxide were used as IPD. The equivalent oxide thickness of each IPD film is equal.

Table 1 Prepared samples for this study

Sample	Floating gate	IPD
A	Ultra-thin floating gate	Single Oxide
B	Conventional floating gate	Single Oxide
C	Conventional floating gate	ONO

3. RESULTS AND DISCUSSION

3.1 Cross Sectional View

TEM cross sectional view of the thermal oxide films on the ultra-thin floating gate electrode and the conventional floating gate electrode are shown in Photo 1 and 2, respectively. The thickness of the both thermal oxide films are 13nm. Photo 2 shows that the conventional poly Si has bumpy surface which may degrade the quality of the oxide films as IPD. On the other hand, the upside surface of a re-crystallized ultra-thin poly Si is so flat as shown Photo 1 that it can improve the oxide quality and may enable to use a single layer thermal oxide film as IPD for flash memory.

3.2 Electrical characteristics

(1)Program characteristics

Fig 1 (a)-(c) show the programming characteristics of the samples A-C, respectively. In the conventional floating gate electrode, the programming speed of samples B and C are not difference from each other although the Vth of sample B is saturated. In the ultra-thin floating gate electrode, the floating gate potential over the drain (Vfd) is higher than that over the source (Vfs) as explained in Fig 2 because the floating gate electrode is fully depleted. Therefore the programming speed of sample A is several times faster than others. [3]

The Vth saturation of the samples A and B can be understood that the FN tunneling current from floating gate to control gate through the single layer thermal oxide film become almost the same as the hot electron injection current from the channel to the floating gate as shown in Fig 3. At the beginning of programming, the FN current is much lower than the hot electron injection. With the increase of Vth by programming (i.e..the decrease of floating gate potential), the FN current increase until the Vth saturation occurs.

The saturated Vth value of sample B is about 4.5V and this small value indicates that a single layer thermal oxide on the conventional poly Si has difficulty to use as IPD. The saturated Vth of sample B is about 6V and large enough for reading. It shows clearly that the smooth surface of the ultra-thin floating gate electrode improve the oxide quality.

(2)Gate disturb characteristics

It is expected that the charge retention characteristics may be the most critical issue of the cells with the single oxide film as IPD because of its leak current. To study this, the gate disturb effect for programmed cell was examined. Fig 4 shows the positive gate bias disturb of the samples A-C, respectively. In samples A and B the Vth degradation are observed. As well as the programming characteristics, sample A is superior to sample B. It is possible to use the structure of the thermal oxide film/ultra-thin floating gate electrode under the condition of Vcg=10V for programming operation although the reduction of control gate voltage down to 8V is needed in order to avoid the gate disturb problem perfectly.

In order to compare the charge loss characteristics with the I-V characteristics between floating gate to control gate, the leakage current was calculated on assumption that the retained charge of programmed cell leaked from floating gate to control gate by the positive gate disturb effect. The results are shown in Fig 5. In sample B, a good agreement with the leakage current of a thermal oxide film on the conventional poly Si which measured with the flat inter-poly capacitor is observed. Therefore the positive gate disturb effect is caused by the FN tunneling current from the floating gate to the control gate through the single thermal oxide film. The leakage current of sample A is two figures lower than that of sample B. It can be said that an ultra-thin floating gate electrode improve the oxide quality.

To compare the thermal oxide film on the ultra-thin Si film with the tunneling oxide, we measured the negative gate disturb characteristics using sample C as shown in Fig 6. This disturb shows the leakage of charge from the floating gate electrode to the Si substrate through the tunneling oxide. At Vth=5V, the electric field of IPD at Vcg=10V is equal to the electric field of tunneling oxide at Vcg=-6.7V. There is no degradation of programmed cell by the FN current through the tunneling oxide. From this data, it can be said that current oxide on the ultra-thin floating gate electrode is not as good as the tunneling oxide and there is a place for a further improvement of the structure of the oxide/ultra-thin floating gate electrode to realize the charge retention characteristics equal to the ONO film.

4. SUMMARY

The possibility of replacing the ONO film to the single layer thermal oxide film was discussed examining flash cell characteristics. The oxide quality on the floating gate electrode was improved drastically by using the ultra-thin floating gate electrode structure. Some application of this structure for flash memory are possible although a further improvement of the oxide quality is preferable.

ACKNOWLEDGMENT

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[2]Y.Yamaguchi et al., Symp. on VLSI Tech. Dig. pp85-86 (1993)

[3]S.Sato et al., Symp. on VLSI Tech. Dig. pp65-66 (1994)

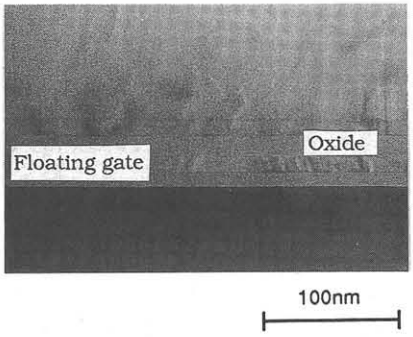

Photo 1 TEM cross sectional view of thermal oxide on ultra thin floating gate

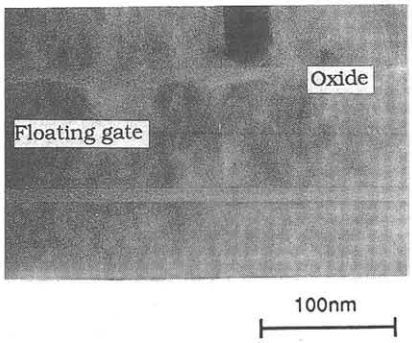

Photo 2 TEM cross sectional view of thermal oxide on conventional floating gate

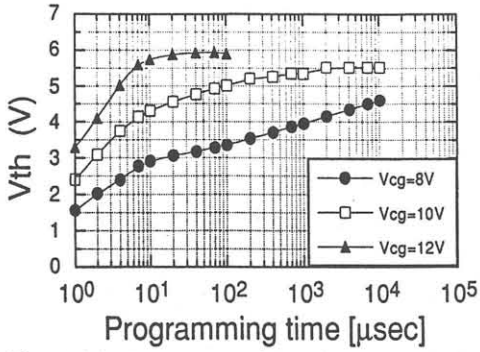

Fig 1 (a) Programming characteristics of sample A

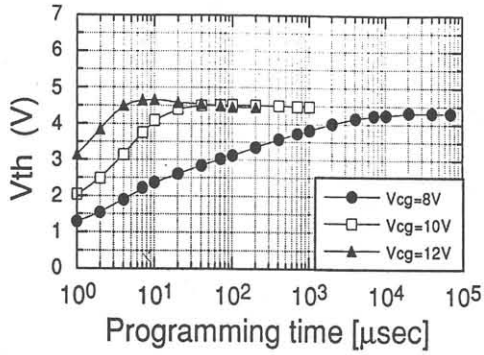

Fig 1 (b) Programming characteristics of sample B

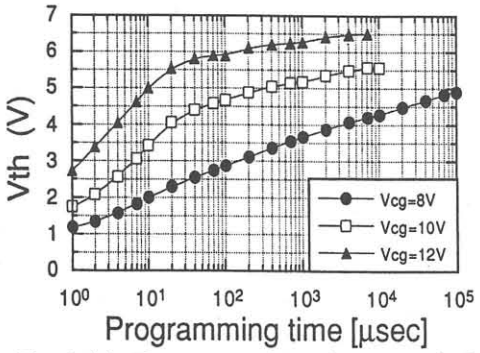

Fig 1 (c) Programming characteristics of sample C

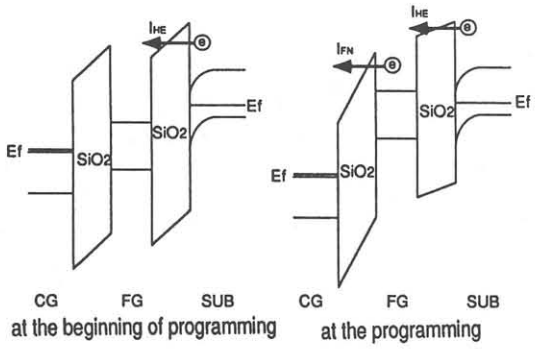

Fig 3 Band diagram of flash memory cell

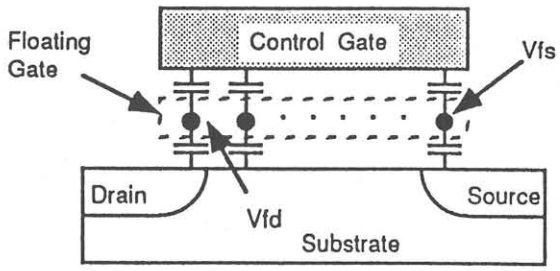

Fig. 2 Model for non-doped poly Si operation
Vfd> Vfs (during programming)

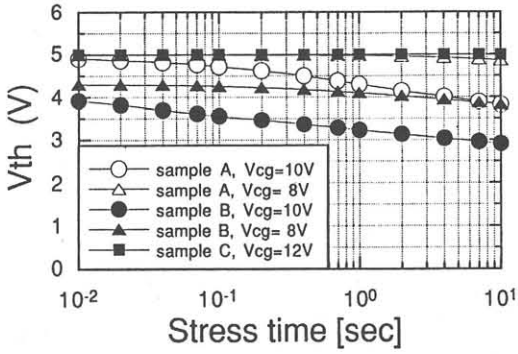

Fig 4 Positive gate disturb characteristics of smples A-C

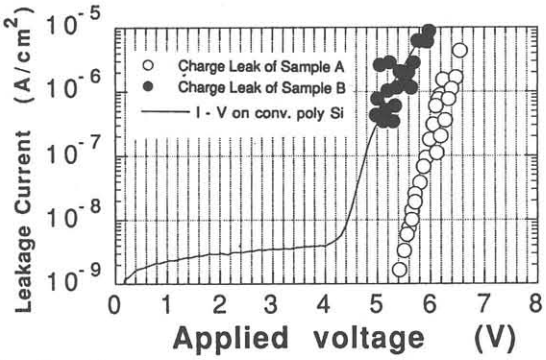

Fig 5 Charge Leak characteristics of sample A and B by positive gate disturb

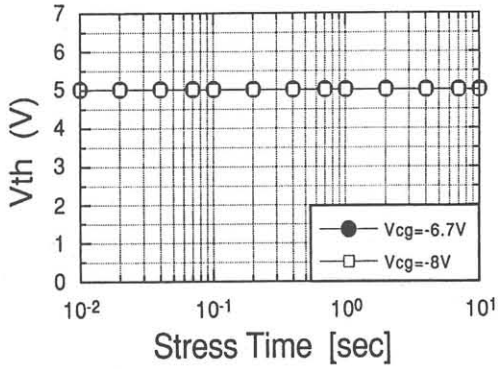

Fig 6 Negative gate disturb characteristics of sample C