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Suppression of Boron Penetration in pMOS by Using Oxide Gettering Effect in Poly-Si Gate

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A new stacked poly-Si gate structure with a thin (~ 20Å) oxide in-between for pMOSFET application is proposed and demonstrated. Due to the gettering fluorine effect of this thin oxide for BF_2^+-implanted poly-Si gate, the concentration of fluorine in gate oxide is decreased. As a result, the enhancement on the boron penetration by fluorine is reduced. And also, this new gate structure improves the electrical characteristics significantly as compared to the conventional one and the stacked layer poly silicon gate structure without a thin oxide in-between.

1. Introduction

As for the submicron CMOS technology, p^+ poly-Si gates are commonly recommended for pMOSFET's to prevent the short channel effect[1]. However, the boron used to dope this p^+ poly-Si gate is easy to penetrate through the gate oxide into the underlying Si substrate, especially for the BF_2^+-implanted poly-Si gate. This will cause reliability problems of devices, such as the positive shift of the threshold voltage, the increment of the gate oxide electron trapping rate, and the p-channel inverse subthreshold slope. Fluorine in gate oxide will enhance boron penetration[1]. Previously, we had proposed a stacked poly-Si gate structure to suppress the boron penetration effectively due to the gettering of fluorine and boron by the interfaces of stacked poly-Si layers[2]. In this work, the effect of fluorine which is easy to segregate at oxide or defect region during annealing process[3] was used to further suppress the boron penetration. A thin oxide is intentionally grown in-between the poly-Si layers of stacked gate structure. Because this thin oxide can getter fluorine and consequently reduce the amount of fluorine in gate oxide, the enhancement on boron penetration by fluorine can be reduced. And due to the less fluorine, consequently, less boron at the gate oxide[4], which results in a better integrity of the oxide, and the relaxation of the stress force between the poly-Si gate and gate oxide by the interfacial oxide inserted in-between the stacked poly-Si layers, the electrical characteristics are much improved.

2. Experimental

The p^+ poly-Si gate MOS capacitors were fabricated on (100), 5~10 Ω-cm, n-type Si wafers with a 80Å gate oxide. The gate oxide was grown in diluted dry O_2 (O_2/N_2=1/6) at 900°C and annealed in N_2 at the same temperature for 15 min. After that, The P^+ poly gate was fabricated by depositing 100nm polysilicon layer and chemically (H_2O_2/H_2SO_4=1/3, 120°C, 10 min) growing a thin oxide (~ 20Å) on the top of the layer and then depositing another 200nm polysilicon layer (POP structure). For comparison, the single layer polysilicon gate (P structure) and the double-layer polysilicon gate but without the chemical oxide (PP structure) capacitors were also fabricated. The total thickness of the gate was 300nm for all the samples. The capacitors were implanted with BF_2^+ at 50 KeV of a dose $5x10^{15}cm^{-2}$, and annealed at 800°C in O_2 for 30 min first and then at 900°C in N_2 for 10, 20, 30, and 40 min, respectively. After the polyoxide was removed, Al was deposited and annealed at 400°C in N_2 for 30 min to make capacitors.

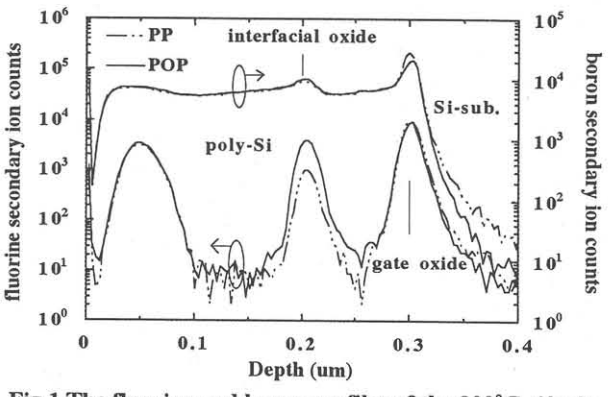

Fig.1 The fluorine and boron profiles of the 900°C, 40min annealed samples PP and POP.

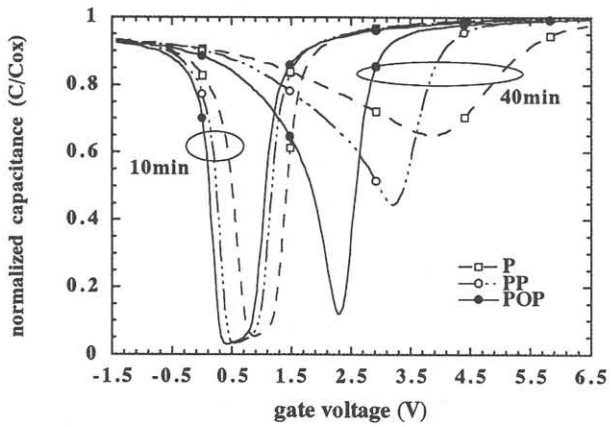

Fig.2 The normalized quasi-static C-V curves for the 900°C, 10min and 40min annealed samples.

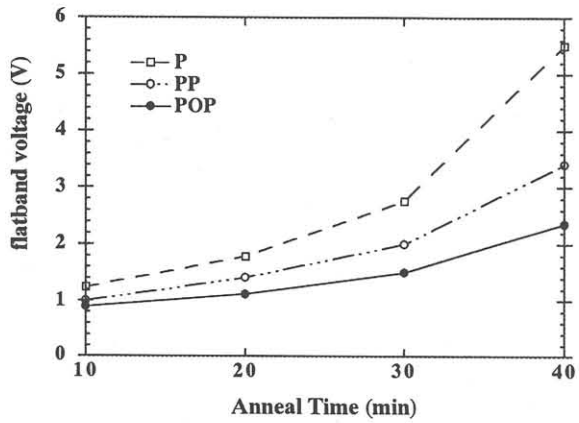

Fig.3 The flatband voltage as a function of the post-implant annealing time at 900°C.

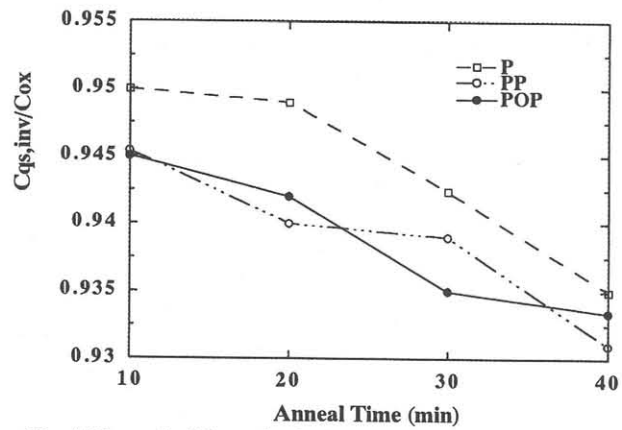

Fig.4 The polysilicon depletion effect, as monitored by the normalized inversion capacitance (Cqs,inv/Cox) as a function of the post-implant annealing time at 900°C.

3. Results and Discussions

Fig.1 shows the SIMS profiles of fluorine and boron for the PP and POP samples after 900°C, 40 min annealing respectively. There are three fluorine peaks, one locates at the region of gate oxide, another is at the interface of stacked poly-Si layers, and the other is at the BF_2^+ implant region. The POP sample has a higher fluorine peak at the middle, where the interfacial chemical oxide is, than that of the PP sample, for which no chemical oxide exists. This thin interfacial oxide getters fluorine and decreases the amount of fluorine in gate oxide, consequently, the enhancement on boron penetration by fluorine is reduced. Thus, the boron concentration of POP sample has a lower peak at the SiO_2/Si interface and a shallower profile in the Si substrate than that of PP sample.

Fig.2 shows the normalized quasi-static C-V curves for the 900°C, 10 and 40 min annealed samples respectively. The POP samples had the C-V curves of a less shift and better shape than those of P and PP samples, which implied that the gettering fluorine effect of this ultra-thin oxide grown in-between the poly-Si gate (POP) suppressed the boron penetration and the formation of boron-related defect centers[5]. Fig.3 shows the flatband voltage (Vfb) shifts with respect to the post-implant-N_2-annealing time for the POP, PP and P samples. The POP samples had the least Vfb shift due to less enhancement on boron penetration by fluorine. Fig.4 shows the ratios of $C_{qs,inv}/C_{ox}$, which are used to monitor the polysilicon depletion effect. The values of $C_{qs,inv}/C_{ox}$ for PP and POP samples were nearly the same but slightly smaller than that of P samples. This is due to that the interface of poly-Si layers can getter boron as well as fluorine and reduce the active boron concentration. The polysilicon depletion phenomenon was not happened in this work for all the samples with different post-implant annealing times, as Fig.2's C-V curves shown.

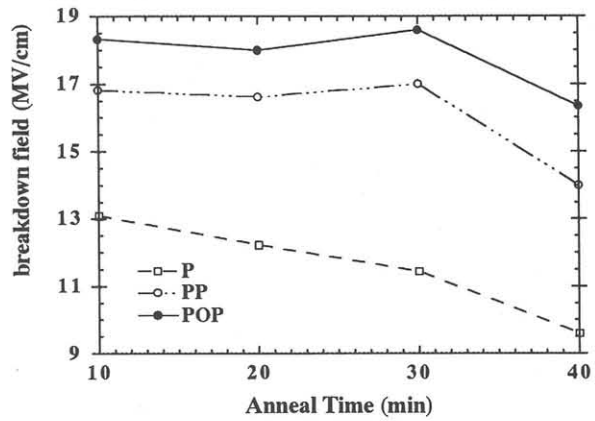

Fig.5 Breakdown field as a function of the post-implant annealing time at 900°C.

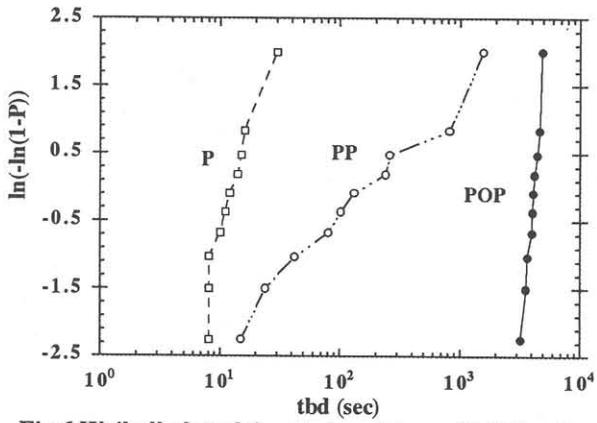

Fig.6 Weiball plot of time to breakdown (tbd) for the 900°C, 10min annealed samples P,PP and POP under constant current ($10mA/cm^2$) stress.

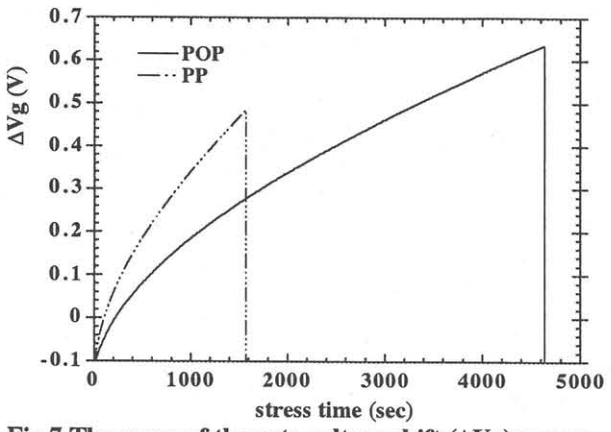

Fig.7 The curve of the gate voltage shift (ΔVg) versus the stres time under the constant current (10mA/cm^2) stress for 900°C, 10min annealed samples POP and PP.

Fig.5 lists the Ebd of the samples annealed for different times. The POP samples had higher breakdown fields than PP and P samples for all annealing time. Fig.6 compiles the Weiball plots of TDDB(time dependent dielectric breakdown) for POP, PP and P samples annealed at 900°C for 10 min. It is seen that POP sample has the much larger breakdown charges (~40 coulomb/cm^2) than those of PP and P samples. Fig.7 shows the Vg shift plots under the constant current (10mA/cm^2) stressing for POP and PP samples. The electron trapping rate of POP is smaller than that of PP. All the significant improvement on electrical characteristics of POP structure were believed resulting from a existing interfacial oxide in-between the stacked poly-Si layers. This layer can trap the fluorine, consequently, less boron penetrate through the gate oxide[4], which sustains a better integrity of the oxide, and relaxe the stress force between the poly-Si gate and gate oxide.

4. Conclusions

Based on the above results and discussions, a thin oxide grown in-between the BF_2^+-implanted poly-Si gate structure can effectively suppress the boron penetration. It's due to the gettering fluorine effect of the interfacial oxide and the reduction of the enhancement on boron penetration by fluorine in gate oxide. And owing to the less boron in gate oxide which preserves the integrity of oxide and the relaxation of the stress force between the poly-Si gate and gate oxide by this interfacial oxide, the electrical characteristics are much improved.

Acknowledgment

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