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Abrupt and Arbitrary Profile Formation in Silicon Using a Low-Kinetic-Energy Ion Bombardment Process

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We have discovered that the carrier concentration in a deposited epitaxial silicon layer is easily controlled by changing the ion bombardment energy during the film growth in the low-energy ion bombardment process. While keeping a perfect crystallinity of an epitaxial silicon layer grown at temperature as low as 350°C, an arbitrary carrier profile has been created in the film. Formation of box-shaped profiles as well as staircase-shaped profiles having very abrupt transitions are demonstrated. The stability of carrier profiles against heat treatments has been investigated.

1. INTRODUCTION

In order to preserve desirable device characteristics for miniaturized MOSFET's, the scaling theory requires the inevitable increase in the substrate doping concentration. The increase in the impurity concentration, however, unavoidably reduces the channel mobility and increases the gate-drain Miller capacitance, thus severely degrading the speed performance of circuits. Since subthreshold leakage characteristics are improved by modifying the vertical impurity distribution, limitations of normal operation for miniaturized devices have been conquered so far by implementing two-dimensional impurity depth profile, such as deep channel ion implantation, LDD structure, etc. In particular, a box-shaped dopant profile having large concentration region right beneath the surface channel provides the long-channel behavior for deep submicron devices, without degradation in the speed performance due to increased junction capacitance and reduced mobility. Although the advantages of this structure are confirmed by simulations[1], it has been very difficult so far to realize such abrupt carrier profiles by conventional techniques. The ion implantation provides only Gaussian distributions. Since conventional epitaxial growth techniques are usually performed at high temperatures, thermal diffusion spreads abrupt carrier distribution profiles. Thus development of a new process technology to form arbitrary-shaped impurity depth profiles at low temperature is quite essential to realize ultra short channel MOSFET's. The purpose of this paper is to present a unique technology to form arbitrary carrier profiles in epitaxial silicon layers using the high-precision-controlled low-energy ion bombardment process[2]. This new process is based on our new finding that the carrier activation level in the epitaxial film can be changed in real-time during the film growth by controlling the ion bombardment energy.

We have already established silicon epitaxy at temperatures as low as 250°C using an rf-dc coupled mode bias sputtering system[3]. In the process, we utilize concurrent low-kinetic-energy Ar ion bombardment on the growing film surface to enhance surface migration of deposited Si atoms at such a low substrate temperature. Therefore the major factors which dominate the film crystallinity and the electric activity of dopants are ion bombardment energy, ion bombardment flux density, and substrate temperature that determine the degree of surface activation during the crystal growth. Detailed experimental studies on these parameters have allowed us to form desired carrier profiles by means of adjusting the ion bombardment energy under the condition of constant ion flux density and substrate temperature.

2. EXPERIMENTAL

The rf-dc coupled mode bias sputtering system used for this study has been discussed previously[2]. The sputtering target was phosphorus-doped n-type silicon with impurity concentration of $3\text{-}5\times10^{19}\text{cm}^{-3}$, and epitaxial layers were grown on p-type (100) silicon substrates. The p-n junctions formed at the surface can electrically separate the deposited layer from the

substrate, making electrical measurement of epitaxial layers possible. Argon gas pressure of 10mTorr and excitation frequency of 100MHz were employed.

The carrier concentration and the carrier mobility were evaluated by Hall measurement. Carrier depth profiles were obtained by repeating the anodic oxidation and the four-point probe measurements. The crystallinity of as-deposited films and those after thermal annealing was investigated by reflection electron diffraction analysis.

The deposition was performed with various values of ion bombardment energy at constant ion bombardment flux and substrate temperature. The ion bombardment energy was independently controlled by the dc bias voltage applied to the wafer. The typical values of Ar^+ flux and Si deposition rate were 9.8×10^{15}ions/cm^{2}sec and 1.6×10^{15}atoms/cm^{2}sec (20nm/min), respectively, and the substrate temperature was 350°C.

3. RESULTS AND DISCUSSIONS

Figure 1 shows the carrier concentration and the carrier mobility of films grown at 350°C as functions of the ion bombardment energy. For ion energies lower than ~5eV, the mobility becomes smaller as the ion energy decreases. This indicates that lack of total energy supply to the growing film surface results in a poor film quality, which was confirmed by reflection electron diffraction analysis. On the other hand, when the ion bombardment energy is higher than ~5eV, the carrier concentration decreases with the increase in the ion bombardment energy. The substantial increase in the carrier mobility is due to the decrease in the ionized impurity scattering. Within this region of the ion bombardment energy, the carrier concentration can be controlled by the ion energy while keeping the best crystallinity of epitaxially grown films.

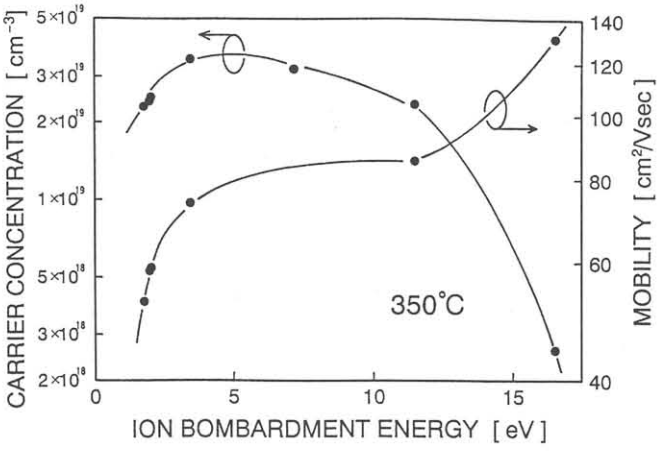

Fig. 1 The carrier concentration and the carrier mobility as functions of the ion bombardment energy. The substrate temperature was 350°C.

The ion bombardment energy was changed from 16.5eV to 7.2eV, and again back to 16.5eV during a single deposition cycle as shown in **Fig.2(a)**. The resultant carrier depth profile is demonstrated in **Fig.2(b)**. A very steep box-shaped carrier concentration layer is realized in the epitaxially grown silicon film corresponding to the pulse-shaped transition in the ion bombardment energy. The data fluctuation observed at constant energy regions is due to the accuracy of the measurement technique. The real value of carrier concentration would be the one indicated by broken lines. It is proved by reflection electron diffraction

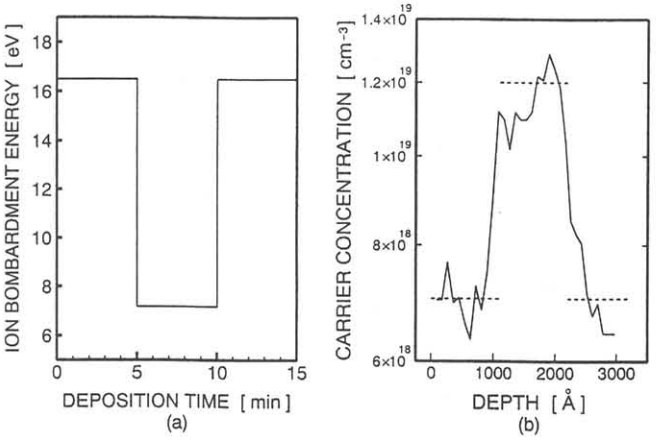

Fig. 2 (a) Temporal change of the ion bombardment energy. (b) Carrier depth distribution of the deposited epitaxial film.

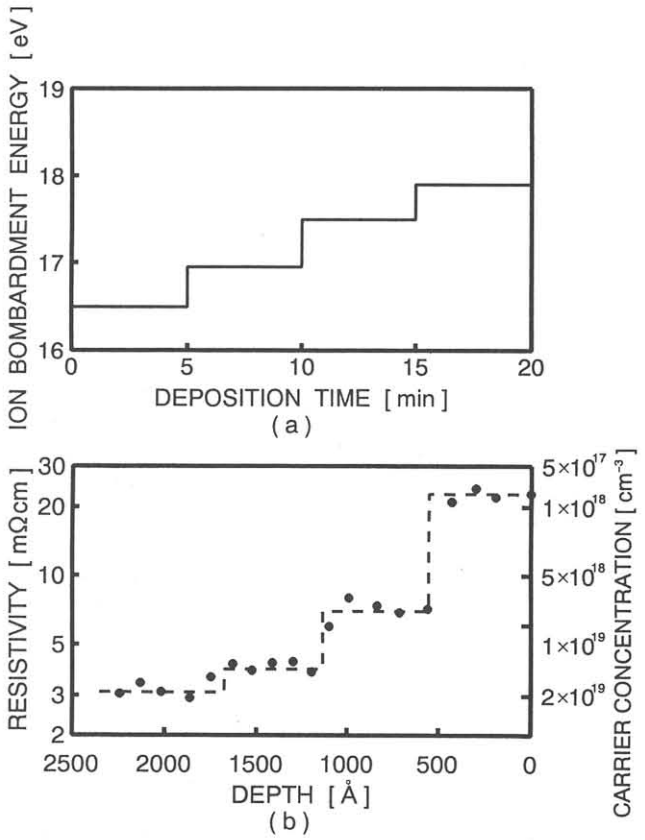

Fig. 3 (a) Staircase transition of the ion bombardment energy. (b) Resistivity depth profile of formed silicon film.

analysis that the formed layer is a single crystal. From these results, we can conclude that the carrier activation level can be controlled by the ion bombardment energy. Carrier distribution in the grown layer can be controlled accurately by the temporal change in the substrate bias voltage that determines the ion bombardment energy. The box-shaped profile below the channel region, which is easily formed at low temperature with this deposition technology, is very promising to overcome the short channel effects without degrading the speed performance[1]. **Fig.3(b)** demonstrates the staircase-shaped profile formed by the ion energy shift as shown in **Fig.3(a)**, where the ordinate is indicated by both the film resistivity and the carrier concentration. Thus formation of arbitrary-shaped carrier profiles in silicon (e. g., pulse-shape, graded-shape, etc.) can be realized at low temperature with this deposition technology by simply controlling the substrate bias voltage that determines the ion bombardment energy.

Stability of such carrier profiles against heat treatments at varying temperatures were investigated in order to study the compatibility with device fabrication processes. The annealing time dependence of carrier activation at the temperature of 900°C is shown in **Fig.4**. Rapid activation of impurities occurs in about 1 hour at this temperature. The carrier concentration, however, does not reach the impurity concentration of the target silicon of $3\text{-}5\times10^{19}cm^{-3}$. The influence of annealing temperature on silicon layers having various carrier activation levels created by various ion bombardment energies is shown in **Fig.5**. Although the carrier concentration tends to increase as the annealing temperature rises, substantial difference in carrier concentration is still preserved even at 900°C after 5 hours annealing. However the combination of this process and the total low-temperature(<500°C) processing[5,6] is ideal.

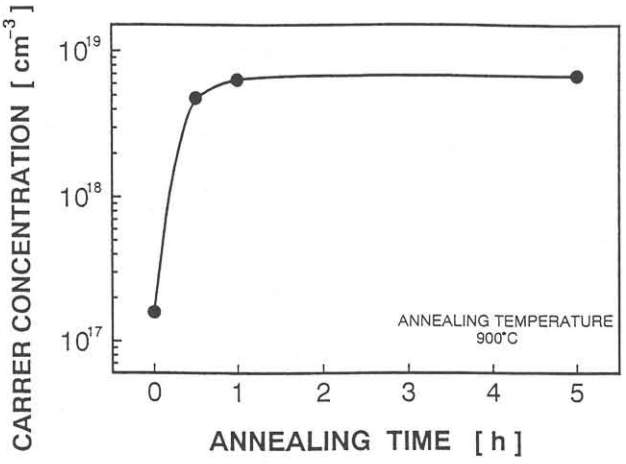

Fig. 4 Relationship between the annealing time and the carrier activity at a temperature of 900°C.

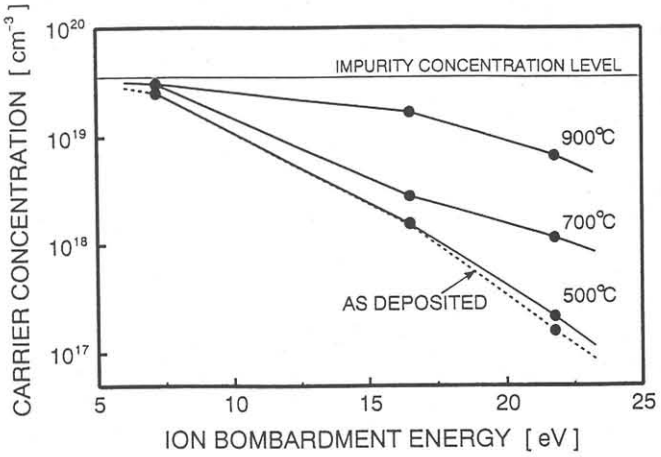

Fig. 5 The annealing temperature dependence of the carrier concentration. Silicon layers having various carrier activation levels were annealed for 5 hours at 500°C, 700°C, and 900°C.

4. CONCLUSION

In this study, the relationship between the ion kinetic energy bombarding the growing film surface and the carrier concentration of the grown layer has been investigated. It has been proved that the carrier concentration can be controlled by the ion bombardment energy in low-energy bias sputtering process. As a result, the formation of arbitrary carrier profiles has been demonstrated. It is known that the box-shaped carrier profile which is easily obtained by this technique is very attractive in the design of ultimately small dimension devices. The formed depth profile is stable under low-temperature processes.

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