## Invited

## **AFM-Based Fabrication of Semiconductor Nanostructures**

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AFM-generated surface modifications are used to fabricate Si nanostructures. We employ the local electric field of a metal-coated AFM tip which is operated in air to selectively oxidize regions of a H-passivated Si surface. The resulting oxide, ~ 2 nm thick, is used as a mask for selective etches of the unoxidized regions of Si. This AFM-based fabrication process is fast, reliable, simple to perform, and is well suited for device fabrication.

The demonstrated ability of proximal probes such as the scanning tunneling microscope (STM) and the atomic force microscope (AFM) to image and manipulate single atoms on a surface suggests that these instruments may surpass the size limits of electron-beam lithography as a nanofabrication tool. However, the application of STM/AFM surface modifications to device fabrication has proven difficult, in part because such probes perform best when modifying very thin layers of material which for the most part are not sufficiently robust for pattern transfer into a semiconductor or metallic structure. Such thin layers are necessary to attain fine resolution with probe tips which act as a diverging source of charge or electric field. This restriction does not apply to conventional electron beam lithography systems which can achieve fine resolution using relatively thick resists by exposing them with a collimated beam of electrons. Thus, the key to practical proximal probebased nanofabrication is the development of thin (i.e. near-monolayer) surface layers which can be chemically modified for use as effective etch masks or growth templates for fabricating semiconductor or metallic structures.

At least two examples of successful pattern transfer using near-atomically thin, chemically-modified surface layers have been reported. In one example, the local electric field of an air-operated STM (or AFM) tip is used to selectively oxidize regions of a Hpassivated (100) Si surface.<sup>1</sup> The resulting oxide is thin (~ 2 nm), yet serves as an effective mask against liquid etching of the unoxidized regions of Si.<sup>2,3</sup> This technique is reliable, simple to perform, and can be extended to other materials such as GaAs.<sup>4</sup> In addition, the technique has been used to fabricate working electronic device structures.<sup>5</sup>

Another example of this type is the use of an ultrahigh vacuum STM to disable the chemical functionality of a self-assembling organosilane monolayer film.<sup>6</sup> This patterned film is then used as a template for the electroless plating of thin Ni films. This technique is promising because the selfassembling films can be attached to many different materials and can have a variety of chemical functionalities.<sup>7,8</sup>

These two examples demonstrate the feasibility of utilizing STM/AFM-modified surface layers for pattern semiconductor and metallic into transfer nanostructures. Due to the local nature of the tipsample interaction and the fact that the chemicallymodified regions are only a few nanometers thick, one can expect fine lateral resolution. In fact, 10 - 30 nm resolution has been demonstrated in both of the above cases. In addition, near-atomic resolution has been achieved for Si surface oxidation when the exposure process is performed in ultra-high vacuum.9 These examples show that proximal probes such as the AFM and STM are rapidly becoming viable tools for nanofabrication.

STM/AFM-based surface oxidation of Si has been investigated by a number of researchers. Dagata, *et al.* were the first to report the STM-induced oxidation of a

H-passivated Si (111) surface.<sup>1</sup> Since then several related studies have been published by a number of researchers.<sup>10-13</sup> Perhaps most notable of these are the atomic resolution results of Lyding *et al.* mentioned above.<sup>9</sup>

While STM-induced surface oxidation is a simple and reliable process, its success depends on finding an application for such a thin oxide. Our own work has concentrated on the use of these surface oxides as a mask for pattern transfer by selective liquid etching.<sup>2</sup> In addition, we have expanded the fabrication process to other materials such as GaAs<sup>4</sup>, extended the exposure process to the AFM<sup>3</sup>, fabricated working electronic devices<sup>5</sup> and micromachined free-standing wires and cantilevers.<sup>14</sup>

Our success in pattern transfer and nanofabrication can be attributed to the ease and reliability of the exposure process and the high selectivity of certain chemical etches. This combination of reliable chemical surface modification and effective pattern transfer makes this a model system for STM/AFMbased nanofabrication.

The sample preparation procedure we use is a UVozone cleaning<sup>15</sup> of (100) Si wafers followed by a dip in a 10% aqueous HF solution. The sample is then blown dry and mounted in an ambient STM or AFM. The surface oxidation is accomplished by exposing selected regions of the surface to a negatively biased STM or metal-coated AFM tip. 4 - 5 V is normally used for exposure with write speeds up to 10  $\mu$ m/s. Much faster write speeds ~ 100  $\mu$ m/s can be accomplished with higher tip bias.

An AFM image of an AFM-generated oxide pattern is shown in Fig. 1. The AFM image was obtained immediately after writing using the same tip that wrote the pattern. The act of imaging does not expose the surface nor does it damage the existing oxide pattern. The height of the oxide is about 1.5 nm and the period of the grating is 120 nm. The bottom section of the pattern was written at 1.5 V while the top section was written at 2.5 V. All lines were written at the same scanning frequency, so that the longer lines correspond to a higher write speed. The shortest lines were written at 1  $\mu$ m/s while the longest lines were written at 10  $\mu$ m/s.

Note that the oxide pattern is easily observable and is much more pronounced than the background roughness of the surface. This latent image allows the success or failure of an exposure to be determined prior to etching. For example, the pattern written at 1.5 V was marginally exposed while the pattern written at 2.5 V produced smooth continuous lines.



**Figure 1:**  $5 \mu m \ge 5 \mu m$  AFM image of a 120 nm pitch oxide pattern written by the AFM.

Fig. 2 shows an AFM image of the same pattern after etching 10 nm into the surrounding Si with an 11 molar KOH solution. The pattern is faithfully transferred by the selective etch except in the underexposed regions which were written at 1.5 V. Thus, inspection of the oxide pattern can accurately predict which portions of the pattern will withstand the etch. The apparent roughness observed on some of the etched lines is due not to irregular exposure or etch roughness but to debris left behind by the etch solution.



**Figure 2:**  $5 \ \mu m \ x \ 5 \ \mu m$  AFM image of the pattern in Fig. 1 after the surrounding Si has been etched to a depth of 10 nm.

Fig. 3 is a detailed image of some closely spaced etched lines. The figure shows, from bottom to top, a single etched line and pairs of lines which are spaced center-to-center by 40, 30, 20, and 15 nm, respectively. The linewidth is  $\sim$ 20 nm. Note the uniformity of the etched lines and the lack of any proximity effects for such closely spaced features.



**Figure 3:** 0.8 µm x 0.8 µm AFM image of lines formed by etching 10 nm into the Si

This nanofabrication process is easily incorporated into a device fabrication procedure. As an example we have fabricated side-gated Si transistors out of SIMOX. SIMOX is produced by implanting Si with a heavy dose of oxygen and annealing to form an electronic-grade layer of SiO<sub>2</sub> buried below the Si surface. This buried oxide layer isolates wires fabricated on the top Si layer from the underlying substrate.



**Figure 4:** AFM image of a side-gated Si transistor fabricated with the AFM from a 40 nm-thick Si layer which resides on a 300 nm-thick  $SiO_2$  layer which rests on a Si substrate. Both the wire and the gate are attached to contact pads formed by optical lithography.

A side-gated transistor fabricated from such material is shown in Fig. 4. This particular structure was formed from SIMOX with a 40 nm-thick top Si layer. The wire and the gate are attached to larger bond pads (not shown) which were formed by optical lithography. This structure acts as a transistor by using the electric field of the lateral gate to control the conductivity through the wire. In addition, both the carrier concentration and the carrier type of the wire can be independently controlled by backgating the Si substrate.

These examples and others demonstrate the practical application of STM/AFM surface modification for semiconductor nanofabrication. The combination of reliable chemical modification of a thin surface layer and effective pattern transfer make this a model system for proximal probe-based lithography.

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