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Invited

SOI Technology for Low Power Logic Applications

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Abstract

The achievement of high performance CMOS Logic at Ultra Low Power suppliers of 1V or less will require significant advancements in submicron device architectures and design. In both these areas the introduction of new materials such as Ultra thin Silicon on Insulator (SOI) substrates and low dielectric constant materials will play key roles in reducing parasitic capacitances thereby dramatically reducing power dissipation. This paper will review the recent developments in SOI materials, device designs and manufacturing requirements.

Introduction

The emerging low power battery operated applications demand intensive computation and communication capabilities in portable environments. It has generally been recognized that the technology best suited for meeting these system requirements is scaled CMOS due to its high density and low power attributes. However, conventional scaled CMOS has several limitations in the simultaneous achievement of high speed and Ultra Low Power. It has been recently shown {1} that scaled CMOS undergoes drastic reductions in circuit speed as the power supply is scaled below 1V. This is primarily due to the difficulty in scaling threshold voltages to low values without sacrificing drive and off-state leakage. The loss in drive capability is further compounded by the interconnect load capacitances (including parasitics) which fuhrer degrade speed and also increases power dissipation. Consequently the development of scaled CMOS suitable for Ultra Low Power dissipation with reasonable speed will require careful technology tradeoffs in both device design as well as the choice of dielectric materials for interconnects. These developments provide significant boost in performance by reducing **parasitic capacitances** in both device architecture as well as Interconnect performance. Reductions in parasitic capacitances are the key to achieving Ultra Low Power dissipation without sacrificing circuit speed. There are 3 major sources of power dissipation in CMOS circuits:

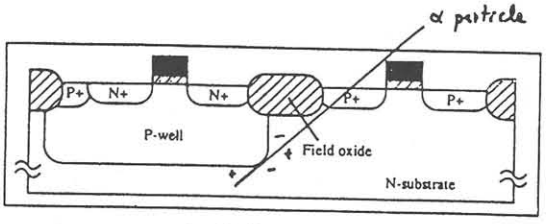
$P_{total} = (C_L V_{dd}^2 f_{clk} N_g) + (I_{sw} V_{dd}) + (I_L V_{dd})$

The first term represents this switching component of power where C_L is the total load capacitance including parasitics, f_{clk} is the clock frequency, V_{dd} the power supply (and logic swing) and N_g the number of simultaneously switching gates. If can be seen that concomitant reductions in C_L (ie parasitics) are essential to reduce P total as V_{dd} is scaled below 1V. The second component is due to the switching transition and can only be controlled by V_{dd} reductions. The third component is the off-state power dissipation due to device leakage (I_L). This component can be significantly reduced by using Ultra Low threshold voltages ($V_t \leq 0.2$ V) with low subthreshold swing ($S < 70$mV/decade) thereby drastically reducing I_L. Thus there are 3 key approaches to reducing power dissipation in scaled CMOS: (i) reduction in parasitic capacitances in both device and interconnects (ii) reduction in threshold voltage ($V_t \leq 0.3$ V) and (iii) reduction in subthreshold slope ($S < 70$mV/dec).

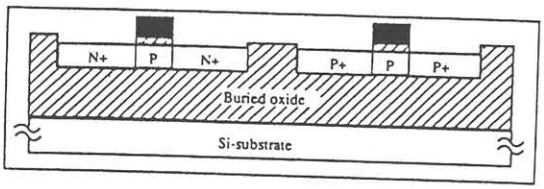
Device Architecture Considerations

The major source of parasitic capacitances in scaled MOS devices are the source/drain junction capacitance, well to substrate capacitance and fringing field capacitances. Fig 1 compares 2 promising device architectures with bulk (a) that significantly reduce parasitic capacitance under the source/drain junctions and also achieve lower subthreshold swings by channel doping profile control under the gate. The first approach CMOS/SOI uses fully depleted silicon-on-insulator substrates that not only simplify the process steps and thus

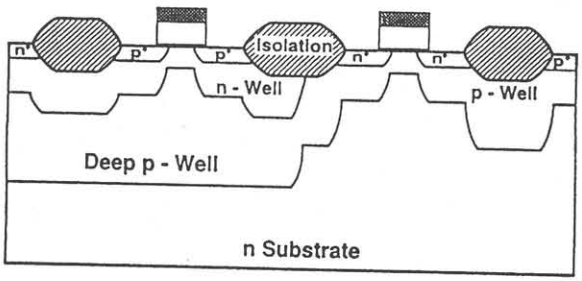
manufacturing cost but significantly reduce parasitic capacitances in the source/drain junctions by the introduction of the "built-in" insulator and the depletion volume below it. By adjusting the channel doping so that the gate depletes through the entire silicon file to the back interface, the channel capacitance is drastically reduced and this improves the subthreshold swing S to below 65mV/dec.



A. Bulk



B. Thin-Film SOI



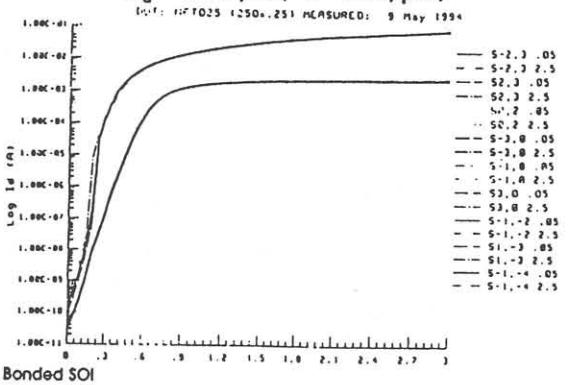
C. CMOS/SJFET

(Fig 1)

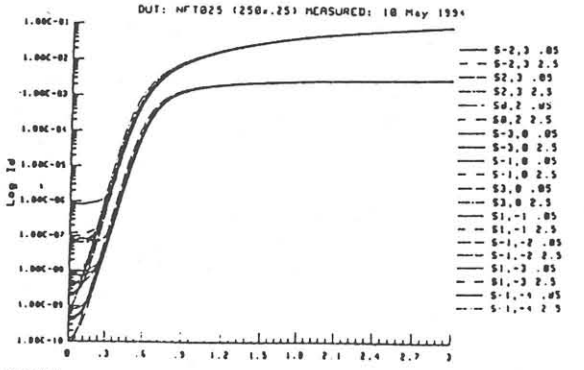
Fig 2 shows data comparing subthreshold turn-off characteristics of 0.25μm bulk CMOS vs CMOS/SOI. It is seen that fully-depleted SOI offers one of the lowest subthreshold swings achievable in scaled CMOS. The second approach CMOS/SJET uses a Vertically Modulated Well doping profile to simultaneously reduce source/drain junction capacitance and channel depletion capacitance under the gate. This profile is achieved through the use of high energy implanted wells that modulate the doping in both vertical and horizontal directions. Data (3) indicates that the SJET device architecture improves both circuit speed and power dissipation over conventional bulk CMOS due to reduction in junction capacitance and subthreshold slope. However the main drawback with the SJET is the large body-factor due to its retrograde doping profile.

Detailed comparison with experimental data will be presented in the paper.

SUBTHRESHOLD CHARACTERISTICS: BULK - VS. SOI
(L_d ~ 0.25 µm / W~ 250/µm)



(A) Bonded SOI
(t_s ~ 1500A°; FD)



(B) BULK SI

(Fig 2)

SOI Materials

The design of high speed transistors in ultra thin SOI structures is primarily dictated by the thickness, uniformity, and material quality of the Si film. But the underlying oxide also has a very important influence on device behavior at submicrometer dimensions. The buried oxide must be of very high quality and thickness uniformity. Under full depletion through the lightly doped SOI film, the transistors become very sensitive to charges at the "back interface" and oxide. This can lead to parasitic "back channel" effects. Some type of substrate bias almost becomes a requirement to maintain control of the off-state leakage and punchthrough. With scaling, the problem becomes aggravated and may even necessitate the use of an additional power supply with higher voltage levels for back bias. Good circuit design and self-aligned processing techniques may potentially circumvent the problem by providing doped regions under both transistor types, thus allowing for substrate biasing of both polarities using the available power supplies. Substrate back-biasing for fully depleted ultrathin SOI designs must be factored into any overall technology/circuit design assessment.

Device scaling of nondepleted ("thick" film) SOI structures requiring high channel doping ($\sim 10^{17}$ cm^{-3}) would closely follow the conventional bulk Si approach, but without the necessity of using substrate biasing for back interface control. Three different approaches are currently used to provide SOI materials for commercial CMOS or bipolar fabrication.

The most popular of these is separation with implanted oxygen (SIMOX) which involves the implantation of a high dose ($\sim 10^{18}cm^{-2}$) of oxygen followed by high temperature annealing. SIMOX provides ultrathin Si films, ~800 to 5000Å thick. Average uniformity is -+ 7% which is adequate for robust transistor design. SIMOX is less flexible regarding the buried oxide layer thickness. The latter is restricted to ~5000Å depending slightly on the implant dose. Such an oxide layer thickness is not ideally suited for low capacitance designs. At present, the Si film quality is also limited by dislocation densities of $\sim 10^4 cm^2$ thereby preventing bipolar applications. Considerable effort is being directed toward reducing this value in order to control process induced defects in manufacturing. Residual heavy metal contamination from the implanter is under control but levels have not been reduced to those for bulk Si with gettering. Scalability to wafer diameters ≥ 200mm is also currently under investigation but the cost is still undetermined.

The bonded wafer technique is a second materials approach. This technique involves the thermally assisted bonding of two oxidized wafers and the careful thinning of one down to the desired thickness by grinding, polishing, and chemical etching. It offers wide flexibility in choosing the Si and underlying oxide films and is also the most cost effective SOI fabrication process, with good scalability to large diameters. At present, the material quality of both the Si and oxide films is virtually identical to high quality bulk Si in defect density and impurity content. The main drawback of the bonded technique is the present inability to produce ultrathin Si films (i.e.; thickness $< 1\mu m$) with good uniformity. While $1\mu m$ is adequate for bipolar and BiCMOS, submicrometer CMOS/SOI requires the development of advanced thinning processes (with etch stops, etc.) to produce films ~1000Å ($0.1\mu m$) thick with thickness uniformities of -+ 5%. Bonded wafer work is currently in progress in both the USA and Japan and progress is likely.

Zone melt recrystallization (ZMR) is the third approach. It involves the recrystallization of an undoped polysilicon layer on top of a high quality, thermally oxidized, bulk Si wafer. The technique offers some flexibility in the design of both the Si film and the oxide but materials problems occur for Si film thickness ~3000Å or less. Film quality is presently defect limited by subboundaries and threading dislocation (thereby preventing bipolar application) and reliability and yield especially at submicrometer dimensions. In addition, the high temperature processing could lead to flatness and warp difficulties at larger diameters.

Summary

This paper has provided a brief overview of the recent developments in SOI device design materials that can significantly impact the development of Ultra Low Power CMOS tailored for the portable computing applications. Detailed tradeoffs on the technical and cost issues will be presented.

[1] A.P. Chranha Sekaren et al, IEEE J.SSC, Vol 27, Nov 4 (1992)
[2] M. Nagata, IEEE J. SSC, Vol 27 Nov 4, (1992)
[3] S. Mori et al, IEDM Digest (1992)
[4] T. Seidel et al, Electro chem Society Symp, 5/1994