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Void-Free Bonded SOI Substrates for High Voltage, High Current Vertical DMOS Type Power ICs

Tomohiro Hamajima Kenya Kobayashi* Hiroaki Kikuchi Kensuke Okonogi
Kenichi Arai Yasuhito Ninomiya* Mitsuasa Takahashi*
ULSI Device Development Laboratories
*Semiconductor Division
NEC Corporation, 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan

Abstract

New structures for intelligent power ICs were developed by using a wafer bonding technique. In these structures, the surfaces of a poly-Si layer and a crystalline silicon wafer are bonded; this combination of bonding surfaces leads to void-free bonding. The electrically perfect bonding at the vertical DMOS region of the new structure was obtained by diffusing impurity into the poly-Si layer. These results indicate that intelligent power ICs can be manufactured by using the new structure substrates.

1. Introduction

A type of intelligent power IC is composed of vertical output devices (VDMOS: Vertical Double-diffusion MOSFETs) having high current and high breakdown voltage capability and low voltage control circuits on a single chip. This integration realizes high performance, reduction in size and high reliability of electronic equipment using power devices. In this structure the isolation method between the VDMOS region and the control circuits region has been key technology. To achieve the perfect device isolation, DI (Dielectric Isolation) has an advantage of protecting the control circuits from high drain voltage of VDMOS, and realizes no latch-up action.

Ohoka et al. have proposed a DI structure by using a wafer direct bonding technique for the fabrication of an intelligent power IC, in which VDMOS and control circuits can be formed [1]. Figure 1 shows a schematic cross-sectional view of the direct bonded structure for intelligent power ICs. In this case the crystalline silicon (c-Si) surface of the base wafer and the coexistent surface which consists of c-Si and Si oxide are bonded. The control circuits region over the oxide film has an SOI structure. However it is difficult to obtain a void-free bonded interface, since the coexistent surface can not be polished as flat as a mirror surface. We observed many voids over the direct bonded wafers by X-ray topography. The voids cause particle contamination from its burst, crystal defects or contact resistance degradation of the bonding interface. To reduce the voids on the bonded interface, micro roughness on the coexistent surface must be less than 20 nm.

In this paper, we propose new DI structures for the fabrication of intelligent power ICs by using a wafer bonding technique in which poly-Si and c-Si are bonded. We show that this bonded wafer enables us to obtain a void-free bonded interface and has an electrical contact suitable for VDMOS region of intelligent power ICs.

2. Structure

Figure 2 shows the schematic cross-sectional view of the new DI structures named PSB (Poly-Si Sandwiched Bonding) structure, in which a poly-Si layer lies between an active layer and a base wafer. In this structure the coexistent surface is covered by poly-Si. The bonding surfaces are poly-Si and c-Si of the base wafer. Since it is easy to polish the poly-Si surface as a mirror bonding surface, the void-free bonding can be obtained.

There are two methods of the lateral isolation between the VDMOS region and the control circuits region. The lateral isolation method is determined by the drain voltage of VDMOS cells and the device fabrication cost. Figure 2-(a) shows the PSB structure with DI type lateral isolation. Another type of isolation is JI (PN Junction Isolation) type lateral isolation shown in Figure 2-(b).

The fabrication process flow is shown in Figure 3. (1) First, flat recesses are formed on an N- type Si substrate. The depth of recess is about 1 μ m. Next, an oxide film is formed by thermal oxidation. (2) The oxide film is polished up to the point where c-Si be-comes exposed on the VDMOS region, and then the coexistent surface with c-Si and Si oxide is formed. (3) The entire coexistence surface is covered with the poly-Si layer. Then the poly-Si surface is polished so that the surface becomes as flat as a mirror wafer surface. (4) The poly-Si surface and a low-resistance N+ wafer surface is bonded at room temperature and then subjected to a heat treatment at 1100℃ for about two hours in a nitrogen or an oxygen ambient. (5) The N-type substrate is ground and polished to form an active layer. The thickness of the active layer depends on the performance of the VDMOS and the impurity diffusion in the device fabrication process. Then lateral device isolation is fabricated in the device fabrication process. An electrically perfect bonded interface for the VDMOS region is needed so that the drain current of the VDMOS flows vertically through the poly-Si layer and the bonded interface. Therefore, we diffused N type impurities into the poly-Si layer.

3. Experiments and results

3-1 Void-free bonding

We have examined perfectness of the bonded interface of the PSB wafer shown in Figure 3-(5) to confirm the physical bonding. Figure 4 presents the cross-sectional view of the PSB wafer by SEM. This image shows that a buried oxide film and a poly-Si layer are fabricated between an active layer and a base wafer. In the X-ray topography images of the PSB wafer, no void can be observed in contrast to direct bonded wafers. Figure 5 indicates the cross-sectional view of the poly-Si layer and a bonded interface by TEM. As shown in this picture, no micro-void is detected at the bonded interface. These results show that the crystallographically perfect bonding is achieved by PSB structure.

3-2 Electrically perfect bonding

To examine the electrical bonding of the VDMOS region, we fabricated PSB wafers having Si/poly-Si/Si structure without buried oxide films.

We selected phosphorus and antimony as impurities for the poly-Si layer considering the difference in the diffusion coefficients. Figure 6 shows the resistivity profiles of the PSB wafers by means of SR (Spreading Resistance). These samples were measured after the annealing for the bonding. These profiles show that the resistivity of the poly-Si layer is about 1×10^{-2} Ωcm, which is almost equal to that of the base wafers and is low enough to permit the drain current flow. To study the electrical characteristics of VDMOS, we have fabricated PSB wafers that have no buried oxide films and manufactured VDMOS cells on the wafers without lateral isolation. Figure 7 indicates the current-voltage characteristic curve of VDMOS cells on the PSB wafer. In this picture the curve is almost the same as that of VDMOS cells formed on a conventional N/N+ epitaxial wafer. The ON-resistance value is shown Table 1. These results illustrate the electrically perfect bonding is also achieved by the PSB structure.

Next, we examined the diffusion of impurities from the poly-Si layer and the N+ base wafer to the active layer during the heat treatment (1200 ℃, 20 hours). Diffusion length of the impurity during this heat treatment is almost same as the length during the full device fabrication process of the PSB wafer with JI type lateral isolation (see Figure 2-(b)). In this study the thickness of the active layer has been decided about 15 μ m based on the characteristic of VDMOS.

Table 2 shows the impurity diffusion length from the poly-Si layer into the active layer for each impurity. The computer simulation shows that phosphorus diffuses up to the surface of the active layer during this heat treatment. On the other hand, antimony diffuses only about 8 μ m from the poly-Si layer. In the case of antimony, we have actually annealed PSB wafers at 1200℃ for 20 hours, and measured the resistivity profiles by means of SR. The antimony diffusion length by the experiment is almost the same as the length by the computer simulation. These results indicate that after the device fabrication the impurity profile of the PSB structure with an antimony diffused poly-Si layer is suitable for the vertical DMOS type intelligent power ICs.

Summary

A novel poly-Si sandwiched bonding structure has been developed and we have achieved crystallographically and electrically perfect bonding. Thus better intelligent power ICs will be fabricated by the present bonded SOI structure.

Acknowledgment

We are grateful to Mitsubishi material silicon Co. for wafer bonding.

Reference

[1]T.Ohoka et al.: The 5th Internat. Symp. on Power Semiconductor Device and ICs, ISPSD'93 Monterey, California, USA (1993)

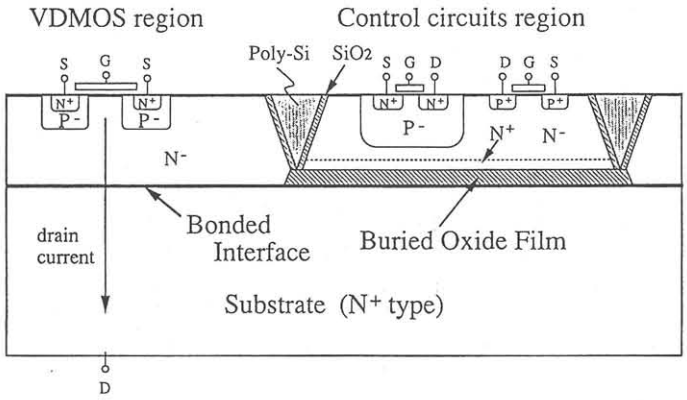
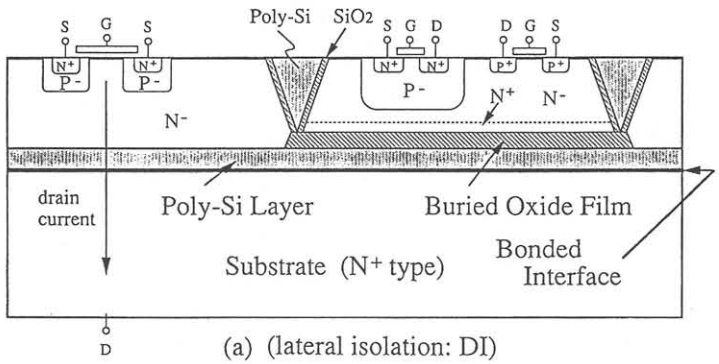
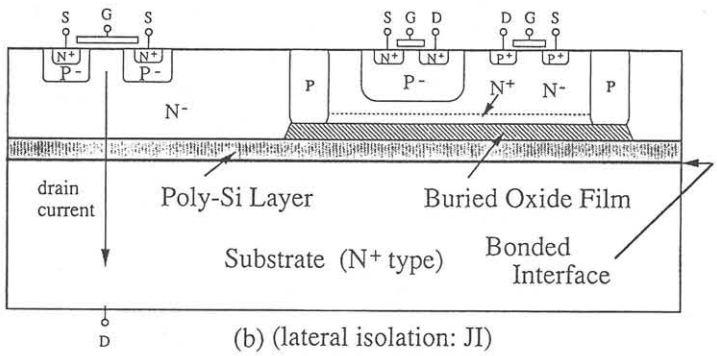


Fig.1 Cross-sectional view of the direct bonded structure



(a) (lateral isolation: DI)



(b) (lateral isolation: JI)

Fig.2 Cross-sectional view of PSB structure

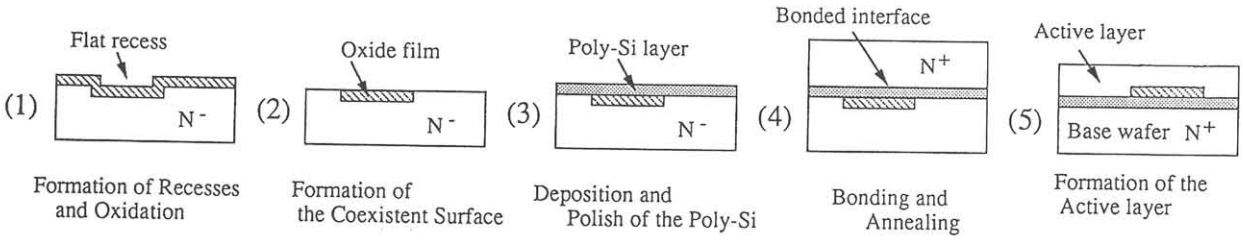


Fig.3 Fabrication process flow of PSB substrate

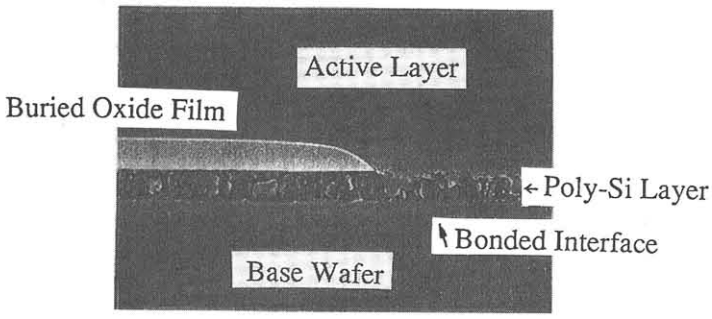


Fig.4 Cross-sectional view of PSB structure

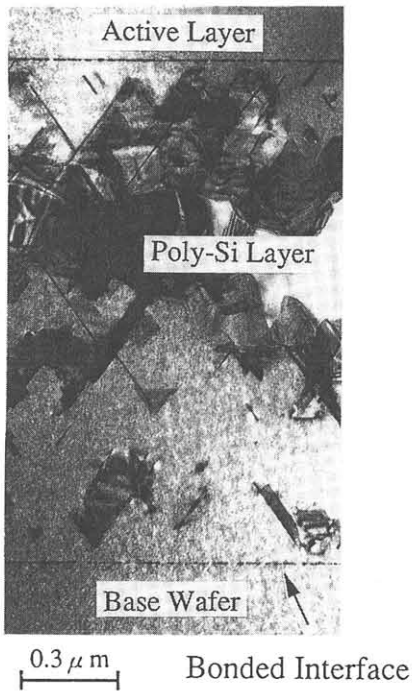


Fig.5 Poly-Si layer and the bonded interface of PSB wafer by TEM

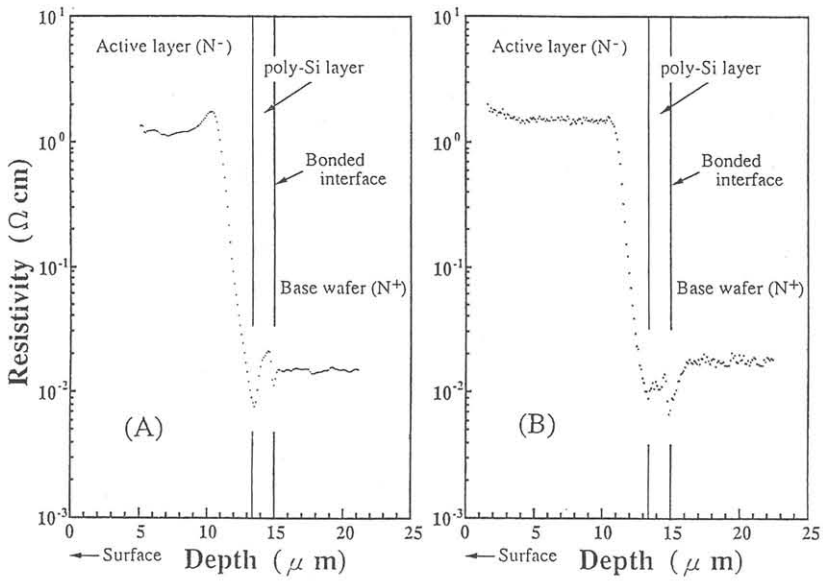


Fig.6 Resistivity profile of Si/poly-Si/Si structure by means of SR

(A) : diffused antimony into poly-Si
(B) : diffused phosphorus into poly-Si

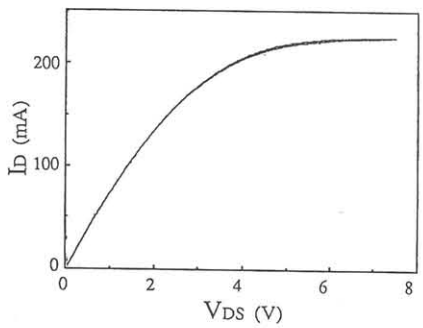


Fig.7 ID-VDS characteristic curve

Table 1 ON-resistance value of VDMOS (Ω)

PSB Wafer			Conventional Epitaxial Wafer		
av.	max.	min.	av.	max.	min.
12.98	13.6	12.4	13.43	14.8	12.2

Table 2 Diffusion length in the poly-Si layer (μ m)

Impurity in the Poly-Si Layer	Computer Simulation (1200℃, 20 hours)	Experimental
Phosphorus	14.4	---
Antimony	8.2	8.0