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Switching Characteristics of a Thin Film SOI Power MOSFET

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This paper describes switching characteristics of a 50-V class thin film SOI power MOSFET based on the results of numerical simulation. It is studied the dependence of the rise time and fall time on the doping concentration of the substrate, on the doping type of the substrate, and on the thickness of the buried oxide layer. In addition, the optimum device structure of the thin-film SOI power MOSFET for high-frequency switching application is also described.

1. Introduction

Silicon-on-Insulator (SOI) technology offers inherent advantages for high reliability, high packing density, high voltage capability, and low thermal generation current.[1] In particular, due to its easiness in fabrication process, thin-film SOI technology has been studied by many researchers trying to develop high-performance power ICs and high-voltage devices.[2),3),4)] The most important objective for power MOSFETs is improving their high-frequency switching performance to reduce the size of electrical equipment as much as possible. Thin-film SOI power MOSFETs have been more useful in such applications because they have much lower parasitic capacitance than power MOSFETs fabricated on a conventional bulk Si substrate. However, not much attention has been given to designing a thin-film SOI power MOSFET suitable for high-frequency switching applications.

This paper describes switching characteristics of a 50 V thin-film SOI power MOSFET based on the results of numerical simulation. In addition, the optimum device structure of a thin-film SOI power MOSFET for high-frequency switching applications is also described.

2. Simulation Method

A schematic cross section of the simulated thin-film SOI power MOSFET is shown in Fig. 1, where T_{box} is the thickness of the buried oxide and T_{ox} is the gate oxide thickness. A heavily n^+-doped poly-Si gate is used as a gate electrode. The body contact was formed during numerical simulation. The main device parameters are listed in Table 1. The specific on-resistance ($R_{on} \cdot A$) and the breakdown voltage (BV_{dss}), rise time, and fall time were numerically studied using MEDICI, a two-dimensional device simulator which solves Poisson and carrier continuity equations.[5)]

3. Simulation Results and Discussion

The main simulated static characteristics of the thin-film SOI power MOSFET are listed in Table 2. The impurity concentration of the drain offset region (N_{off}) was chosen to be the optimum dose,[4)] which achieved the highest breakdown voltage for each T_{box}. Here, BV_{dss} and $R_{on} \cdot A$ are almost constant regardless of the substrate type and impurity concentration of the substrate (N_{sub}). Also, $R_{on} \cdot A$ and BV_{dss} decrease as

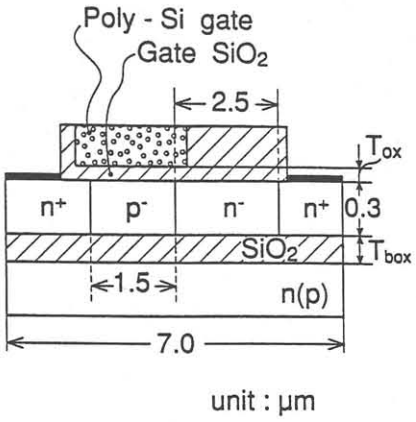

Fig. 1 Schematic cross section of the simulated thin film SOI power MOSFET.

Table 1 Main device parameters.

T_{box} (μm)	0.2 ~ 1.0
T_{ox} (nm)	50
V_{th} (V)	0.5 ~ 0.6
Substrate	n: 1×10^{19} cm^{-3}
	p: 1×10^{14} cm^{-3}

Table 2 Main device static characteristics.

T_{box} (μm)	substrate type	Ron • A (mΩ•cm²)	BVdss (V)
0.2	n*	1.28	44
	p**	1.29	44
0.44	n*	1.52	62
	p**	1.54	61
1.0	n*	2.23	63
	p**	2.25	63

* n : Nsub = 1.0×10^{19} cm^{-3}
** p : Nsub = 1.0×10^{14} cm^{-3}

T_{box} is decreased.

The dependencies of the rise time and the fall time on N_{sub} are shown in Fig. 2 when T_{box} is 0.44 μm. The rise time and the fall time were simulated by using transient analyses with resistor load circuit. The rise time is almost constant regardless of the substrate type and N_{sub}. The fall time of the p-type substrate is faster than that of the n-type substrate when N_{sub} is less than 1×10^{16} cm^{-3}. The fall time of the n-type substrate is independent of N_{sub}, while the fall time of the p-type substrate decreases as N_{sub} is decreased below 1×10^{16} cm^{-3}. The depletion layer, which spreads into the substrate, is shown in Fig. 3 at the source-to-drain bias of 0 V, for an n-type low resistivity substrate (n-type of N_{sub} $1 \times 10^{19} cm^{-3}$) and a p-type high resistivity substrate (p-type of N_{sub} 1×10^{14} cm^{-3}), respectively. The depletion layer spreads into the substrate region only for the p-type high resistivity substrate. This depletion layer reduces the drain to substrate capacitance (C_{dsub}) and reduces the fall time of thin film SOI power MOSFETs.

The dependencies of the rise time and fall time on T_{box} are shown in Fig. 4. The rise time of the n-type substrate is almost the same as that of the p-type substrate. The rise time of both types of substrate increases as T_{box} decreases. The fall time of the p-type substrate is faster than that of the n-type substrate. The fall time of the n-type substrate increases as T_{box} decreases because C_{dsub} increases as T_{box} decreases. On the contrary, the fall time of the p-type substrate nearly does not vary with T_{box} because depletion layer spreads into the substrate region, thereby maintaining the C_{dsub} value regardless of T_{box}.

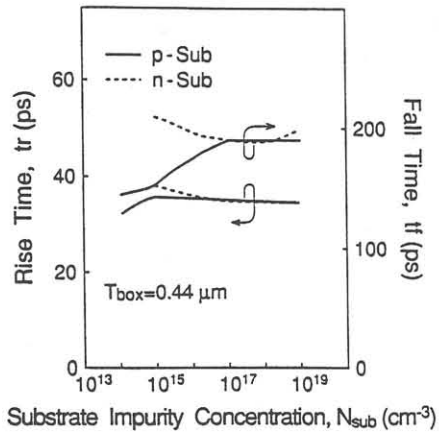

Fig. 2 Dependence of the rise time and fall time on the impurity concentration of the substrate.

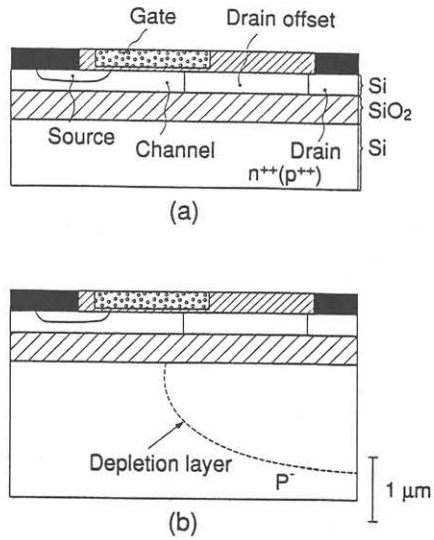

Fig. 3 Cross sectional views of depletion layer spreading into the substrate for (a) n-type low resistivity substrate and (b) p-type high resistivity substrate.

The dependencies of the rise time and fall time of the 1 A-class power MOSFET on T_{box} are shown in Fig. 5. In this case, the rise time and the fall time were numerically simulated by using a resistor load circuit. For numerical simulations, the on-resistance was chosen 1 Ω by adjusting the gate width. The gate width used in the numerical simulation is shown in Table 3. The increase of the gate width can be found as T_{box} increases, because the optimum dose decreases as T_{box} increases. [4] The rise time is faster than the fall time. The rise time increases slightly as T_{box} decreases. The rise time of the n-type substrate is slightly faster than that of the p-type substrate. The fall time of the p-type substrate is faster than that of the n-type substrate. The fall time of the n-type substrate increases as T_{box} decreases thanks to the increase of C_{dsub}. On the contrary, the fall time of the p-type substrate is improved by reducing T_{box} because the gate width

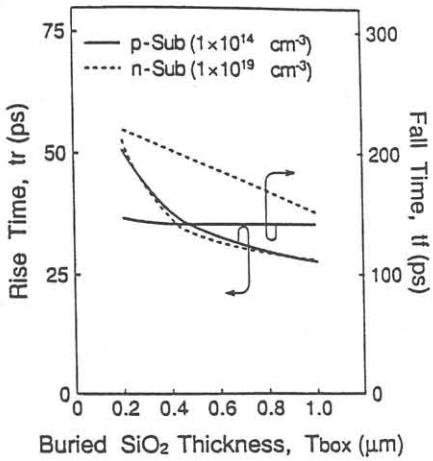

Fig. 4 Dependence of the rise time and fall time on the buried oxide thickness.

decreases as T_{box} decreases, which leads to decrease of C_{dsub}. These results demonstrate that a device structure with the thinnest possible buried oxide layer thickness on p-type high resistivity substrate is preferable for the shortest switching speed considering the breakdown voltage. This tendency is good agreement with our previously reported paper which discussed the specific on-resistance of the thin-film SOI power MOSFET.[4)]

4. Conclusions

The switching characteristics of a thin-film SOI power MOSFET were simulated in order to optimize its structure. The specific on-resistance and the breakdown voltage were independent of the substrate type and impurity concentration of the substrate. The rise time was faster than the fall time. The rise time was almost constant regardless of the substrate impurity type and concentration. The fall time of the p-type substrate was faster than that of the n-type substrate. The fall time of the n-type substrate increased with decreasing in the buried oxide thickness. The fall time of the p-type substrate remained almost constant regardless of the buried oxide thickness. The thinnest possible buried oxide layer thickness with p-type low resistivity substrate should be chosen for getting the shortest switching speed.

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Table 3 Gate width used in the simulation.

Tbox (μm)	Substrate type	Gate width (cm)
0.2	n*	1.83
	p**	1.84
0.44	n*	2.26
	p**	2.28
1.0	n*	3.19
	p**	3.21

* n : Nsub = 1.0 x 10¹⁹ cm⁻³
** p : Nsub = 1.0 x 10¹⁴ cm⁻³

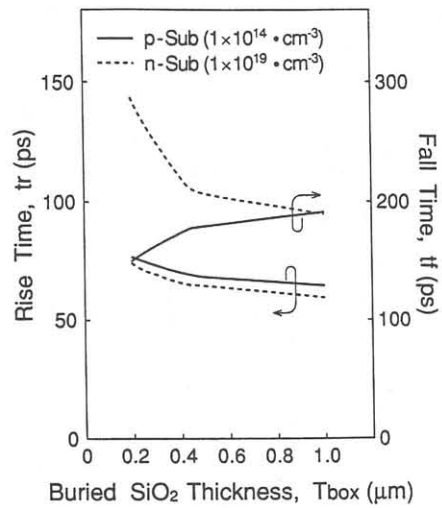

Fig. 5 Dependence of the rise time and fall time of the 1 A-class thin film SOI power MOSFET on the buried oxide thickness.

REFERENCES

1) *Silicon On Insulator For VLSI and VHSIC*, ed G.E. Norman (Academic Press, London, 1982) Vol. 4, p. 1.
2) S. Marchant, E. Arnold, H. Baumgart, S. Mukherjee, H. Pein and R. Pinker: *Proc. 3rd Int. Symp. Power Semiconductor Device & ICs, Baltimore,* 1991 (IEEE, New York, 1991) p. 31
3) T. Matsudai, and A. Nakagawa: *Proc. 4th Int. Symp. Power S emiconductor Devices & ICs, Tokyo*, 1992 (The Institute of Electrical Engineers of Japan) p. 272
4) S. Matsumoto and H.Yoshino: *Jpn. J. Appl. Phys,* Vol. 33 (1994) Pt. 1, No. 1B p .519
5) *TMA MEDICI Two-Dimensional Device Simulation, User's Manual, 1992* (Technology Modeling Associates, Palo Alto, 1992).