Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 256-258

Invited

Advances in the Production of Thin-Film Bonded SOI and Ultra Flat Bulk Wafers Using Plasma Assisted Chemical Etching

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In 1992 a new technique for producing thin, uniform silicon-on-insulator (SOI) films by Plasma Assisted Chemical Etching (PACE) was introduced. During the period since this introduction, advances in the equipment and processing techniques have resulted in significant improvements in SOI film thickness uniformity. The technology has also been extended to several new applications which have the potential for dramatic improvements in the preparation of semiconductor materials.

1. BACKGROUND

Conventional grinding and polishing of bonded SOI wafers can produce film thickness of 1–3 μm nominal thickness with thickness uniformities of 0.5 μm. Although these wafers are suitable for some specialized applications, many potentially high volume applications such as CMOS require film thicknesses of 50–300 nanometers.

In 1992 Hughes Danbury Optical Systems announced the development of the AcuThin® process as a technique to produce thin uniform SOI films from conventionally prepared bonded SOI substrates.[1] The process, shown schematically in Figures 1 and 2, employs a high speed thin-film mapper which measures the film thickness at thousands of points. This data is used to control a spatially confined plasma etch tool to reduce the film thickness and improve the uniformity of the film. At the time of its introduction, the process was capable of producing bonded wafers with film thickness of 100 nanometers with uniformities of ±10%.

2. SOI PROCESS IMPROVEMENTS

Since the introduction of this technique, continuous hardware and software improvements have resulted in improved film thickness uniformity of the thinned SOI wafers. In January 1994 a new fully automated cassette-to-cassette vacuum cluster tool capable of high-volume production of thinned SOI wafers (Figure 3) was commissioned. This tool includes an integrated thin film measurement station having much greater accuracy than the earlier instruments. The superior optical performance of this system in conjunction with the greater process stability inherent in the vacuum cluster tool design has resulted in further improvements in SOI film thickness uniformity. Figure 4 shows the trend in thickness uniformity during the last two years as measured by the standard deviation of the film thickness. Each data point represents the average of a lot of fifty 100 mm SOI wafers.

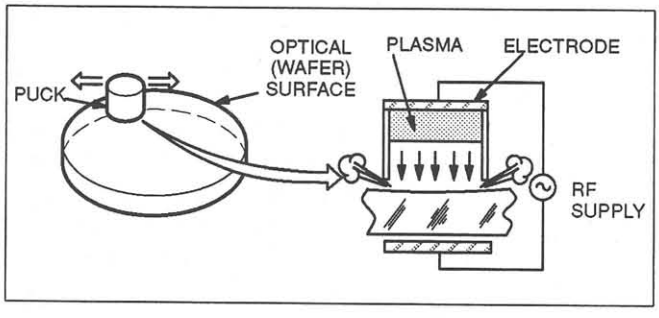

Fig. 1. Plasma assisted chemical etching (PACE).

3. PACE APPLICATIONS WITH OTHER MATERIALS

This process is equally applicable to the thinning of various other SOI structures. Experimental lots of silicon-on-quartz (SOQ) and silicon-on-sapphire (SOS) have been processed in this equipment. The high speed film thickness instrument can be used to characterize a wide range of single and multiple layer film configurations. In the cases of both SOS and SOQ the silicon film thickness was successfully reduced while the film uniformity was dramatically improved.

The thickness uniformity of epitaxial silicon layers can be processed by PACE to improve the thickness uniformity. Experiments have demonstrated the potential of

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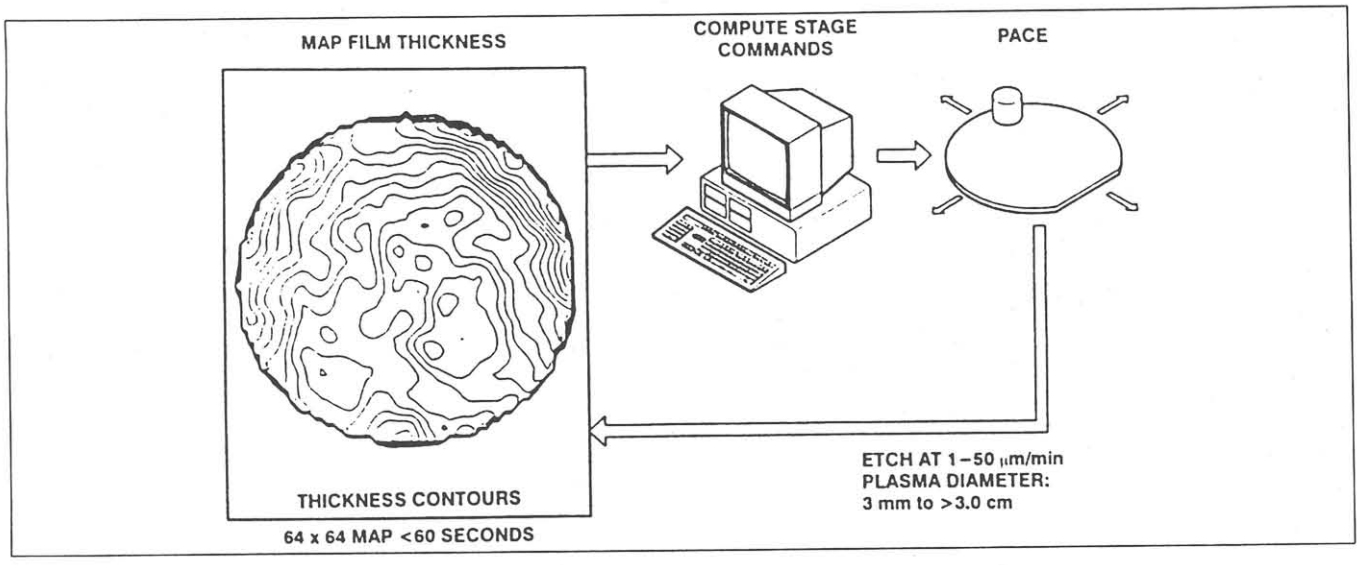

Fig. 2. SOI wafer thinning process.

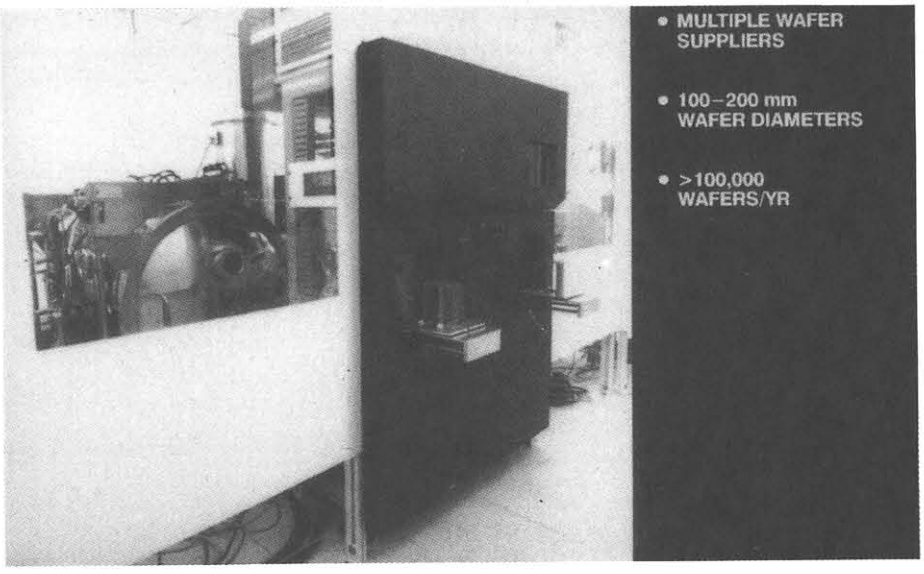

Fig. 3. Production capability.

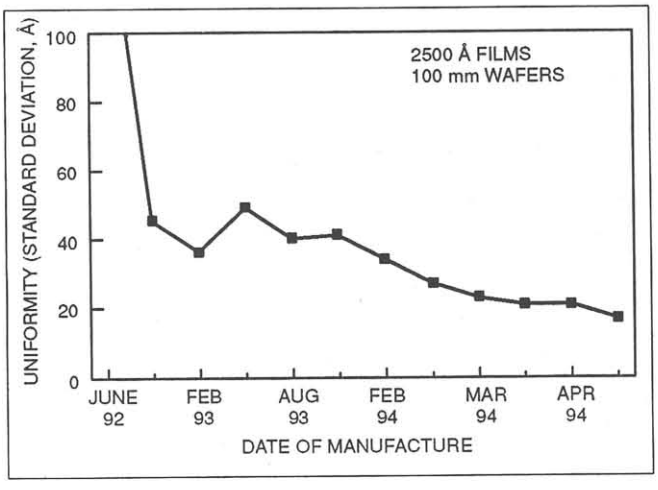

Fig. 4. SOI thickness uniformity: improvement June 1992 – April 1994.

this process on epi layers ranging in thickness from 3–100 μm.

The PACE process is also under investigation for its potential in backside wafer thinning. Potential applications for this technology include CCD array thinning for detector applications and backside thinning of completed ICs for stacking and improved thermal heat sinking. Bulk silicon wafers have been thinned to as little as 10 μm by PACE.

4. BULK WAFER FLATTENING

During the period since the introduction of this process several new applications for the PACE technique in the preparation of semiconductor materials have been under development. The most significant of these new applications is the production of very low total thickness variation (TTV) bulk wafers. Using thickness data obtained from commercially available instruments, the

PACE process can be employed to dramatically reduce the thickness variations in bulk silicon wafers. Figure 5 contains data taken from an ADE Model 9500 thickness gauge for a 200 mm wafer before and after PACE processing. Figure 6 shows site flatness distribution data for a lot of 200 mm wafers before and after PACE processing. Detailed surface analysis has shown that the PACE process, unlike other techniques for creating ultraflat wafers, creates no surface damage requiring further material removal. Several thousand wafers have been flattened with this equipment during the last two years.

5. CONCLUSIONS

During the past two years the PACE process has emerged as an effective technique for producing high quality thin SOI films using bonded wafers. The PACE process has also proven to be a highly flexible technique for improving the quality of SOI and other semiconductor substrates. Numerous new applications have emerged in which PACE is an enabling technology that will facilitate the manufacture of new structures not currently feasible using conventional processing techniques. The potential for cost reduction in wafer processing over conventional processes is expected to be demonstrated in the near future.

6. REFERENCE

1) P. B. Mumola, et. al., IEEE International SOI Conference Proceedings (1992) 152.

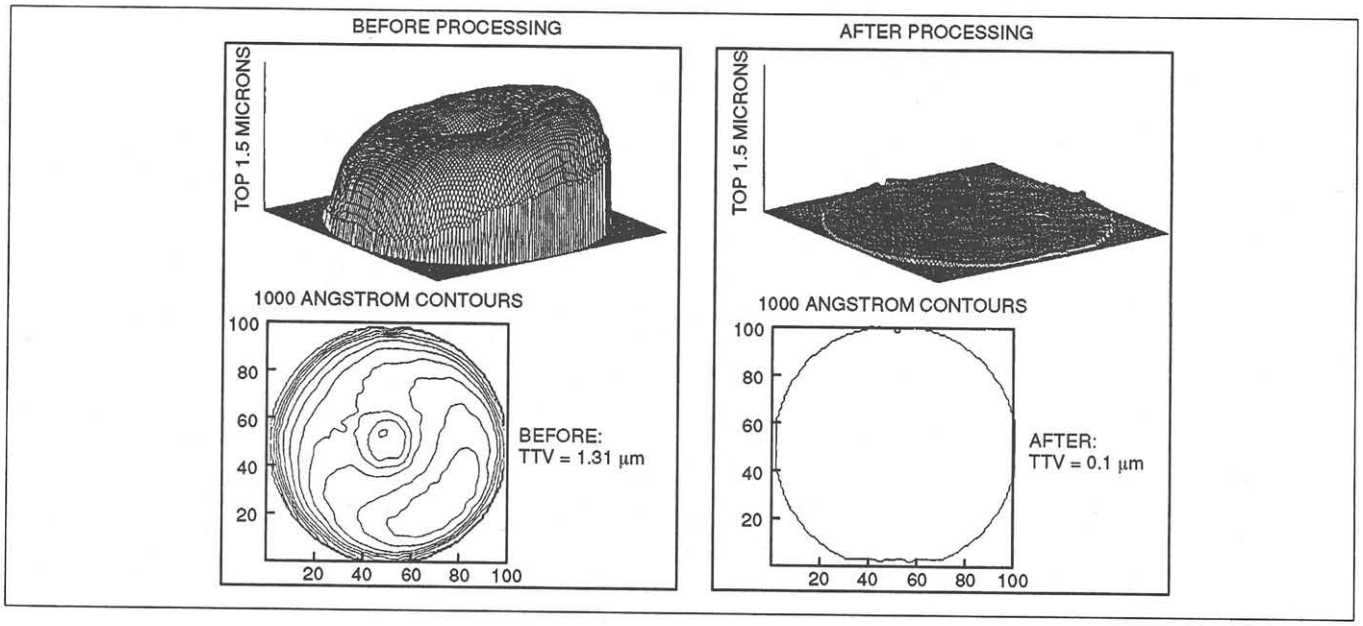

Fig. 5. 200 mm wafer flattening demonstration.

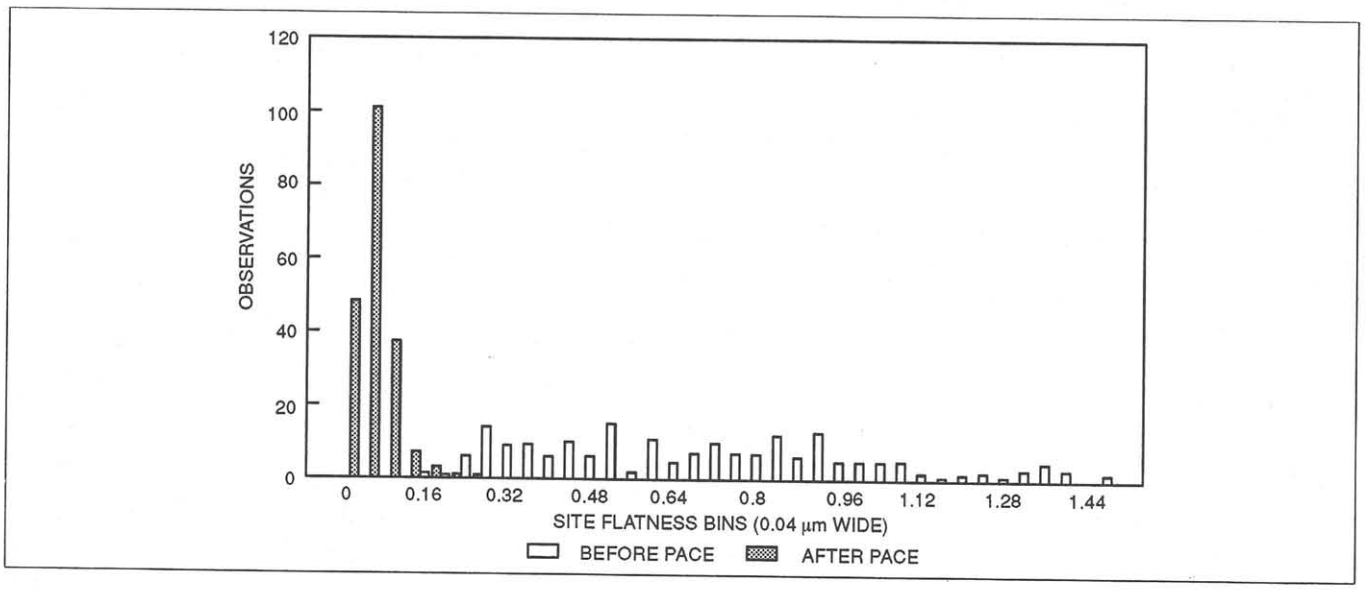

Fig. 6. TTV experiment: site flatness, before and after processing.