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Invited

SOI for Low-Voltage and High-Speed CMOS

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The rise in power of a high performance logic chip that fully utilizes most advanced CMOS technologies is becoming a serious concern for many applications. Ultimately in order to accommodate the chip power, a reduction in chip size, density, and supply voltage is required, which will result in lower system performance. In this paper it is demonstrated that CMOS on Silicon on Insulator (SOI) offers circuits with lower power at the same performance. Undepleted CMOS on SOI technology allows a manufacturable CMOS technology with much improved delay×power and extendible to low 1.X *volt* regime. A 512 Kb SRAM with access time of better than 3.5 nS at 1.X V is demonstrated. Clear power-performance advantage of CMOS on SOI over bulk it the technology of choice for sub-0.25 μm-1.X V CMOS generations.

1- INTRODUCTION

Scaling of CMOS has been the main tool for improving the ULSI system performance over the last two decades. On Figure 1, the relative switching energy of a loaded 3-way NAND in various technologies and maximum reported or expected chip power is shown. Although at every generation there has been a marked improvement in relative switching power, the power of a chip that fully utilizes the speed-density potential of a technology and most advanced CMOS circuit and logic design practices, has increased drastically. It is clear that in addition to the reliability issues, power consumption has to be considered in deciding the elements of a sub-0.25 μm CMOS technology. This will necessitate dropping the voltage faster than required by the reliability requirements, which will result in performance loss. Nevertheless in bulk CMOS, because of its high threshold and body effect, the supply voltage must remain $\geq 1.5V$ in high speed designs. Using SOI, it is possible to obtain lower power×delay values than in bulk CMOS. On SOI, MOS device can have subthreshold slope lower than 60 mV/dec and lower the effective device threshold. This will permit further drop in supply voltage, while preserving the same leakage current and performance, thus leading to lower power.

In this paper the design and technology of a 1.X V, sub-0.25 μm CMOS on SOI is described. This technology is applied to a 512 Kb SRAM with access time of better than 3.5 nS at 1.X V. Clear power-performance advantage of CMOS on SOI over bulk in the sub-0.25 μm-1.X V regime makes it the technology of choice.

II- Sub-0.25 μm SOI CMOS DESIGN

Silicon on insulator has failed to break into the main-stream CMOS mainly because of low nMOS breakdown, complexities of device design and the steady improvements of bulk CMOS. Now with the concerns over power and reduced supply voltages, a window of opportunity for SOI has opened. Probably the single biggest barrier to the introduction of SOI has been the "floating body effects". Using ultra-thin fully depleted films has been the main strategy to reduce the floating body effects. But following a study of various MOS on SOI structures, it was found that MOS devices with source-drain extensions on non-depleted SOI is a very attractive design point [2]. This structure is very effective in reducing the floating body effects because the extensions significantly reduce the emitter and the collector areas of the parasitic lateral bipolar. Use of the thick SOI allows utilization of non-uniform doping and source-drain extensions, which are very effective in reducing SCE. The SOI V_T sensitivity to film thickness is eliminated and threshold can be adjusted simply by changing the film doping. Figure 2 summarizes the simulation result of a 0.1 μm nMOS on ultrathin SOI and on thick SOI with extension-HALO, for the high drain bias [2]. Ultrathin SOI can eliminate

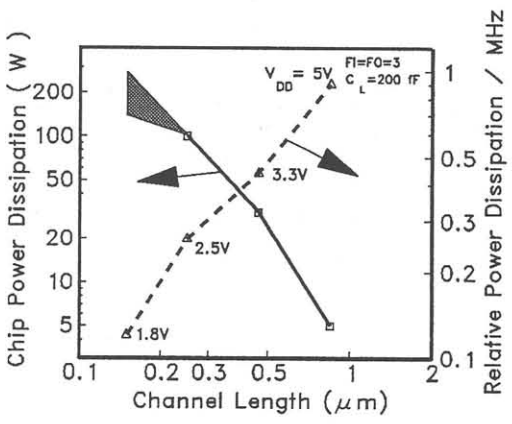

Figure 1- Trends observed in bulk CMOS technology.

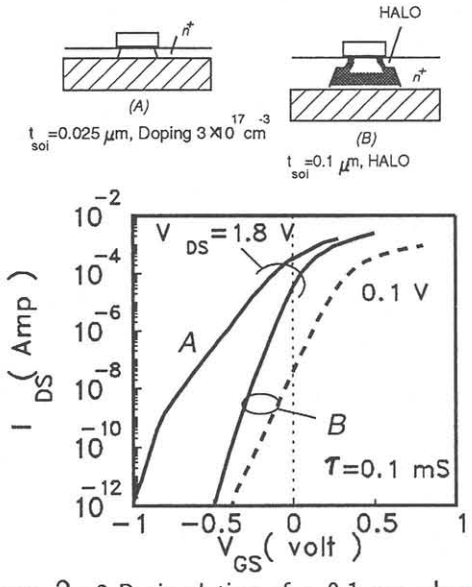

Figure 2- 2-D simulation of a 0.1 μm channel length device on ultra thin and thich SOI (with extension and HALO).

the body effect, but suffers from low threshold and excess SCE. MOS with extension and HALO results in low leakage, and a sub-60-mV/dec subthreshold slope (a consequence of floating body effect). The low threshold in this case can However the kink effect is still present. In digital circuits, the important device characteristics are the on-off currents. Thus the kink effect does not have any effect on the performance of the digital circuits. In fact it leads to more on current. To show that this excess current, which is due to the bipolar device, can be turned on and off quickly and without any long lasting residual currents, simulation of a switching 0.1 μm device was carried out. The gate was turned on and off in 50 $psec$ and the bipolar gain was varied by changing the lifetime. The result is shown in Fig. 3. As the life time is increased, one gets more current as expected, and in all the cases the current reaches its steady state value within 5 $psec$. In cases of analog circuits where high gain in a device is desired, body contact might be used [3].

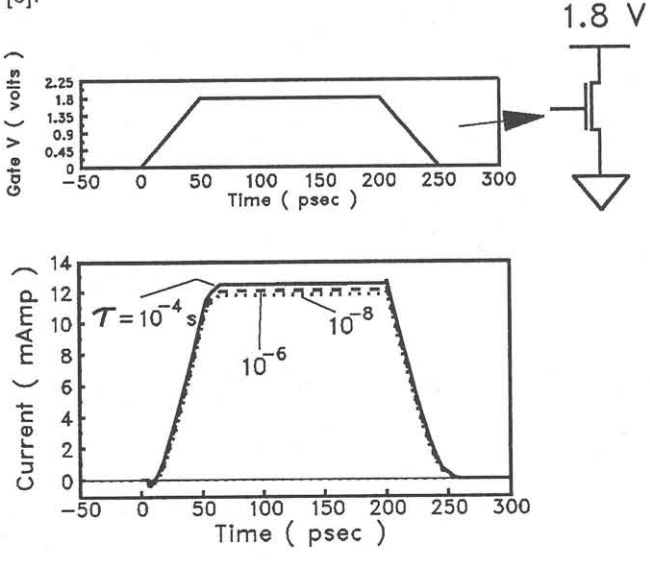

Figure 3- The simulated switching characteristics of a 0.1 μm nMOS on SOI.

III- PROCESS TECHNOLOGY AND ELECTRICAL RESULTS

SOI devices with extension, HALO, non-uniform channel doping were fabricated on relatively thick undepleted SOI (100-150 nm) [2]. Figure 4(a) is the cross section of a finished nMOS device with the drawn channel length of 0.13 μm and the characteristics of the same devices with effective channel lengths of 0.07 μm and widths of 10 μm. Excellent V_T roll-off was obtained. Saturated transconductance on SOI were measured and values similar to bulk were obtained, if the heating during the measurement was avoided [4]. Figure 5 is the switching power per stage of unloaded inverter with 0.15 μm devices on bulk and on SOI. About a factor of 3× improvement in delay-power product is obtained on SOI (This factor is about 2× for 3-way loaded NAND circuits). Improvement in power-delay and low voltage performance of CMOS on SOI are the reasons for using SOI in the deep-submicron region.

IV- CMOS ON SOI FOR 1.0 V APPLICATIONS

Reduction of the power supply voltage in at a given bulk CMOS technology can significantly reduce the chip power but this has usually been accompanied by a large drop in performance. This is due to the reduction of the drive current, the junction capacitance, and the (bulk) MOS body effect. These effects become more significant at lower voltages. Both the body effect and junction capacitance are nearly absent on SOI. SOI operating a 1 V results in significant power×delay improvement as apparent in Fig. 5. When operating at low voltage, it is desirable to drop

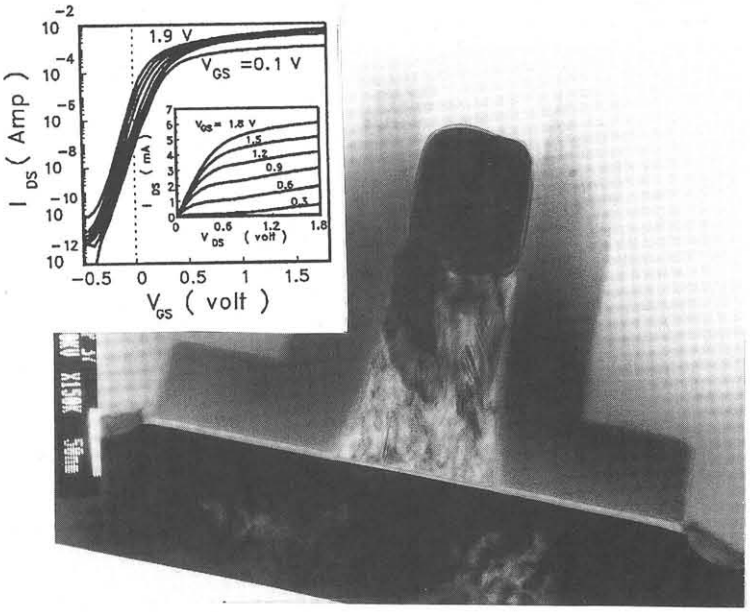

Figure 4- The TEM cross section of a 0.13 μm L_{DRAWN} nMOS on SOI, and the corresponding device characteristics. (0.07 μm L_{EFF}).

the threshold as much as possible: Lower threshold leads to significantly better performance, especially at low voltages. This is shown in Fig. 6, where circuit simulations of loaded 3-way NAND were carried out at different thresholds (L_{EFF}=0.25μm). Lower V_T is also beneficial in reducing the V_T dependence of performance at low voltages. Non-fully depleted SOI is particularly useful in this respect. Devices on non-fully depleted SOI have a sharper high V_{DS} subthreshold slope (in the high 50's mV/dec range compared to high 80's mV/dec for bulk CMOS) and thus allow lower V_T at the same leakage. This reduction in apparent V_T at high drain voltage and increase in overdrive (without the increase in leakage) is particularly useful in a low voltage CMOS. To show the potential of this device design and capability of SOI when operated at low voltage, this technology was applied to a 3 level metal, fully pipelined 512K SRAM [5]. This SRAM has been previously fabricated in a 0.5 μm 3.6 V CMOS technology and an access time of 3.8 ns at 3.6 V had been obtained. Figure 7 is the access time *vs.* the supply voltage for the SOI SRAM. Successful demonstration of SRAM shows the potential of the present SOI device design working at very low voltages at very high performances, and underlies the fact that non-fully depleted SOI is capable of delivering high performance circuits at low supply voltages with significant performance advantage.

It is argued that due to the increase of the chip power to unacceptably high values in sub-0.25 μm CMOS, it is difficult to fully utilize the potential of the bulk technology in the most advanced logic applications. CMOS on SOI allows better power×delay value. A new design point for SOI, which is extendible to sub-0.1 μm range, is reviewed. This design point uses relatively thick non-depleted (0.15 μm) SOI film, highly non-uniform channel doping and source-drain extension-HALO. It was shown that such SOI technology is particularly useful for a 1.0 V range CMOS. This technology was applied to a self-resetting 512K SRAM. Access times of 2.5 ns at 1.5 V and 3.5 ns at 1.0 V were obtained. Concerns about CMOS power and lower operating voltages now allow the SOI to become a serious contender to bulk Si. It is expected that in the sub-0.2 μm family of CMOS technologies, SOI will be the substrate of choice for high performance logic applications.

VI- REFERENCES

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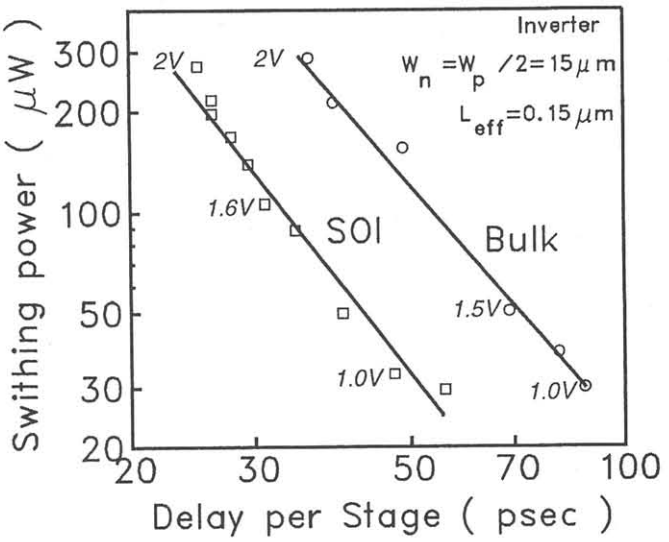

Figure 5- Measured switching power of a single stage Inverter (W_N = 15 μm, W_P =30 μm).

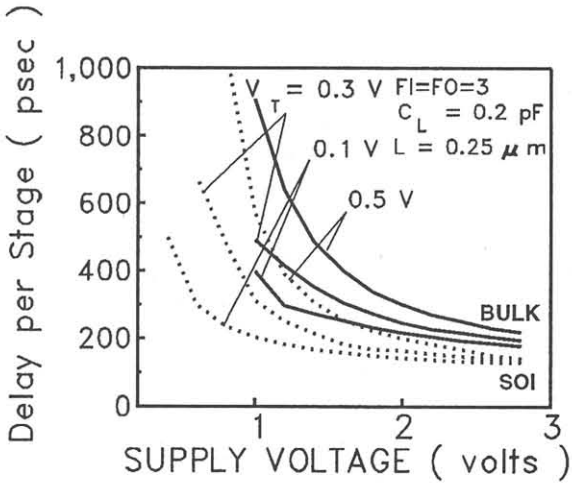

Figure 6- Simulation of fully loaded NAND *vs.* the supply voltage for different thresholds on bulk and on SOI (FI=FO=3, C_L=0.2 pF, W_N = W_P =30 μm at L_{Eff}=0.25 μm).

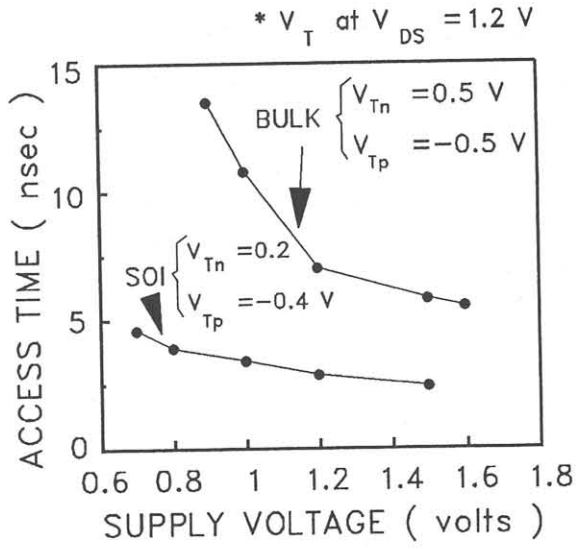

Figure 7- SRAM access time *vs.* supply.