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SOI Technology for Low-Power Applications

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CMOS technology on Thin Film Silicon-on-Insulator(TFSOI) substrate has made significant progress toward a commercially viable technology for low voltage, low power applications[1]. With performance and power advantages over the bulk counterpart demonstrated, a significant part of TFSOI technology effort is now placed on manufacturability and commercialization[2]. The success of commercialization hinges on a strong coupling among materials, device technology, and product definition. Considerations in materials, device design, process integration, circuit design, applications, entry level geometry and reliability will be discussed.
A CMOS technology on SOI substrates at 0.5μm geometry has been established with demonstration circuits ranging from ring oscillators, prescalers, CPUs, and SRAMs showing much improved performance over the bulk CMOS counterpart.
The overall technology characteristics and status with emphasis in manufacturability will be presented.

1. Introduction

TFSOI CMOS technology is compatible with bulk CMOS in many ways ranging from circuit design, layout to wafer processing. The main difference is the device floating body associated with the SOI substrate, and its effects on the device characteristics. This difference results primarily in a reduction of VDD capability for TFSOI devices without modifications such as field shield[3] or body contacts. This prevents a possibility of a mainstream application for power supply at 3.3 V and above, even if all other factors are in place.

The interests in portable and wireless equipment are driving VDD to be lower than 3.3V. This provides an opportunity for TFSOI devices to be introduced as a commercial technology at geometries larger than the commonly believed 0.25 μm.

2. Process Integration

One of the key advantages of the TFSOI process is the high degree of process compatibility with the bulk CMOS counterpart. This greatly simplifies the logistics of the silicon processing, and eases the insertion of a TFSOI process into a bulk CMOS facility.

However, the process integration should not be overlooked. The primary process modules unique to the TFSOI device integration such as salicide[4], and isolation[5] remain challenging. They are coupled strongly to the SOI thickness and uniformity. Great care is needed to ensure manufacturability.

High degree of compatibility in photo, etch, and thermal processes is achievable. The process step reduction[6] is also achievable. The degree of percentage reduction is a function of integration. In general, a 20-30% process reduction can be achieved for a double layer metal process. This allows a reduction in process cost to offset some of the starting wafer cost.

The challenge for the process integration will be higher for smaller geometries which may need thinner silicon thickness. Salicidation on silicon thickness below 1000Å becomes a major challenge in manufacturability. Selective processes in local silicon thinning[7], and raised source/drain[8] have been reported to ease the salicidation difficulty. These alternatives however increase process complexity and cost and therefore negate some of the TFSOI advantages.

3. Device Characteristics

Fully depleted devices have been demonstrated to have better current drive capability over a partially depleted device[1]. However the manufacturability of a fully depleted device is inferior to a non-fully depleted device[2] due to an increase in parametrics sensitivity to SOI uniformity. SOI uniformity and salicidation are major challenges for fully depleted device integration, and parametric control.

The uniqueness of non-fully depleted device characteristics over the bulk CMOS devices is from the floating body effects[1]. These well-known characteristics limit the realization of TFSOI technology for commercialization as much as the material quality and cost. Fig.1a and Fig.1b show typical sub-threshold and output I-V characteristics. The floating body induced body charging results in a higher IDSS and single device latchup as shown in Fig.1a, and low breakdown voltage(Fig.1b). These characteristics set an upper limit of VDD to be typically less than 3.3 V. A direct insertion into 0.5 μm, 3.3 V technology is thus not possible without some form of body contact. The introduction of body contact however complicates the CAD in layout and simulation, and to some extent degrades the performance due to an increase in parasitics. This prevents TFSOI from being a mainstream at 3.3 V and above technology. TFSOI entry for mainstream applications has been

suggested in deep sub-micron (≤0.25 μm) shrink[9] where VDD is expected to be scaled down below 2 V.

However, the growing interests in low power, low voltage[10] have made TFSOI a viable technology at the present geometry due to the power supply reduction. The impact of early breakdown becomes a non-issue.

4. Materials

Although a substantial improvement has been made on the SOI substrate quality and availability, the ability to provide large volume quality material at a reasonable price has not been proven. CMOS circuits at a density of 1/4 to 1/2 Mega bits have been demonstrated[11]. The ultimate question on the SOI materials viability for ULSI remains to be answered[12].

Thin vs. thick buried oxide(BOX) is a point of emphasis from the stand point of material quality and cost[13]. Device design to further suppress short channel effect[13] also favors thin BOX. The penalty in source/drain capacitance and backgate effect can negate some benefits of a TFSOI technology. The trade-off remains to be assessed.

5. Application Considerations

The commercialization of TFSOI technology is limited as much by a proper choice of product, as by material and process technology. As mentioned in the device section, the floating body induced body charging, and early breakdown prohibit the devices to be operated above 3.3 V. The conventional applications for VDD at 3.3 V and above are thus not applicable.

Low power applications require low IDSS and low Vt. Although TFSOI offers a potential improvement in sub-threshold slope, practical device design requirements suggest a nearly fully depleted devices over fully depleted devices. This negates some of the fully depleted device benefits. A much lower Vt expectation from 60 mV/dec is not a practical expectation(Fig.1a).

The lower VDD applications increase the performance sensitivity due to Vt variation as shown in Fig.2. The Vt control is thus more important for low voltage circuits. Unfortunately, on top of all the standard process steps(such as Tox, implant, poly gate length, thermal control, etc.,) which affect Vt variation, silicon thickness variation adds another variable into the Vt variation. It is therefore expected that the Vt control for TFSOI will not be as good as the bulk counterpart.

However, the improved short channel effect and punch-through allow a TFSOI device to be operated at a lower threshold voltage than the bulk CMOS of the same geometry. This also favors a low voltage application for TFSOI technology at the expense of leakage current.

Fig.3 shows a performance comparison on a 1K x 8 SRAM for a TFSOI and a bulk CMOS technologies. The substantial improvement in the memory address access time comes from both the capacitance reduction and "body-effect" suppression. This effect becomes more significant at the lower supply regime. Fig.4 shows the performance data from a divided by 256 prescaler achieved on a CMOS TFSOI technology. A less than 60μW prescaler operated at 500MHz is achieved.

It is plausible that TFSOI technology can be applied beneficially at 0.5 μm providing the operating conditions are adequate. With the emphasis in low power, low voltage[10], TFSOI commercialization has become more desirable.

Some more challenging issues for TFSOI applications are on even higher voltage devices. Portable applications in many cases require embedded EEPROM[14]. High voltage for programming, and erase poses a major challenge to the traditional floating body TFSOI transistors design. Body contact devices offer improved device breakdown. In the limiting case, the body contact devices can achieve the same breakdown voltage. However, this requires layout modification over the conventional device layout. Extra effort in CAD is needed to accommodate the body contact requirements.

6. Summary

CMOS technology on TFSOI substrates has achieved a level where a practical implementation for commercialized is possible. However, floating body limits the application to be less than 3.3 V. Mainstream for 3.3 V power supply is thus not acceptable. Meanwhile, portable and wireless applications open a realm of applications for sub 3.3 V. This allows CMOS TFSOI technology a opportunity for early entry in commercialization. Product definition at low voltage for low power has escalated the SOI applications to a geometry not limited to the "future generations".

References

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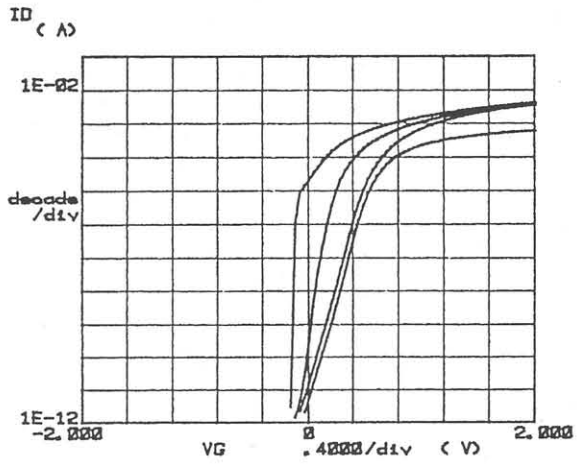

Fig.1a NMOS(Leff = 0.5 μm) Sub-Vt characteristics. VDD start = 0.1 V, step = 1 V. The body charging induced Vt reduction and IDSS increase are negligible at 0.1 and 1.1 V while a much lower Vt and higher IDSS for VDD = 2.1 and 3.1 V.

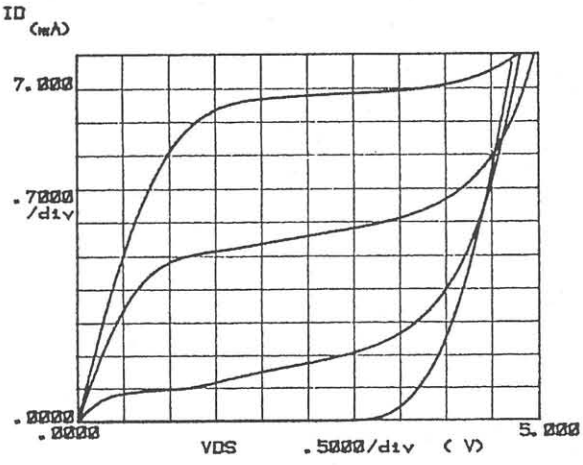

Fig.1b NMOS(Leff = 0.5 μm) IV characteristics. VG step = 1 V. The parasitic bipolar induced early breakdown is at VDS = 3.5 V.

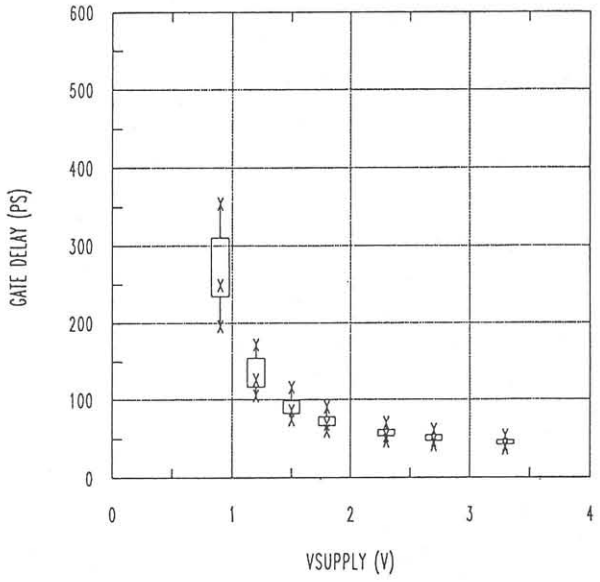

Fig.2 Ring oscillator gate delay vs. VDD. A much large spread in gate delay is seen at lower VDD.

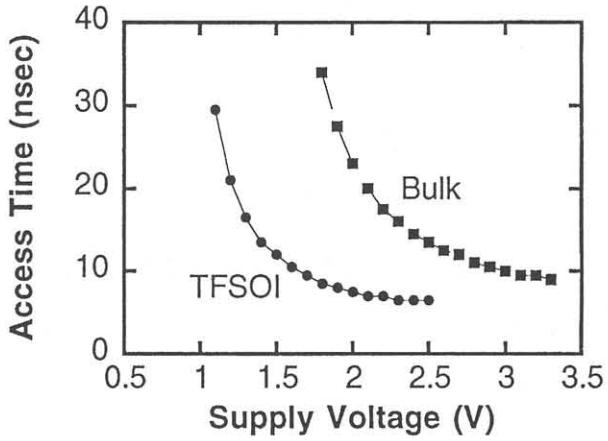

Fig.3 Address access time(TAA) comparison of a 1K x 8 SRAM for bulk vs. TFSOI CMOS.

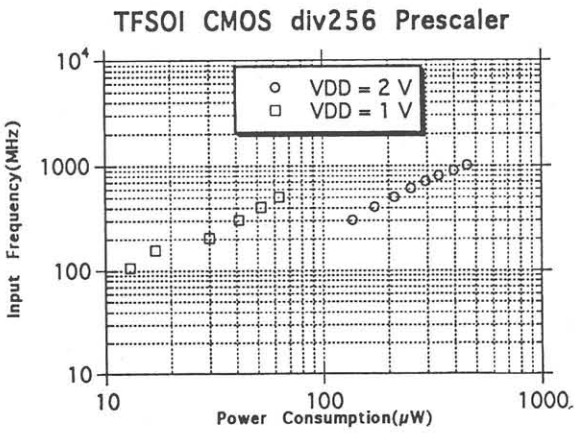

Fig.4 Frequency vs. power consumption of a divided by 256 prescaler for TFSOI CMOS.