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Comparison of Fully Depleted and Partially Depleted Mode Transistors for Practical, High-Speed, Low-Power 0.35 μm CMOS/SIMOX Circuits

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ABSTRACT

We present experimental data concerning the propagation delay time and the power consumption of 0.35um CMOS/SIMOX gates (inverter, NAND, NOR) composed of fully depleted, near fully depleted, or partially depleted transistors with no body-contact, which were fabricated only with our conventional process technologies. On the basis of these experimental data, we address the most essential factors for high-speed, low-power 0.35um CMOS/SIMOX devices.

1. INTRODUCTION

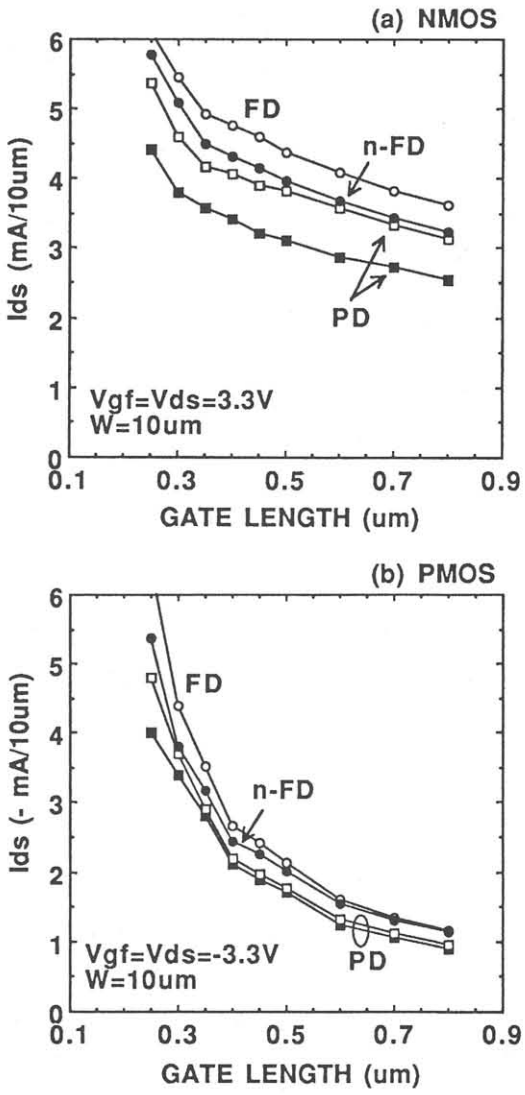
Attractive characteristics of fully depleted (FD) mode transistors have already been clarified [1-3], and high-speed performances of FD mode CMOS/SIMOX devices have also been demonstrated [4-8]. However, essential roles of the fully depleted mode itself for improving performances of CMOS/SIMOX digital circuits have not been shown clearly. In this paper, we present our experimental data concerning the propagation delay time and power consumption of CMOS/SIMOX ring oscillators (inverter, NAND, NOR) composed of fully depleted (FD), near fully depleted (n-FD), or partially depleted (PD) mode transistors with no body-contacts, and discuss the most essential factors for practical, high-speed, low-power CMOS/SIMOX circuits.

2. EXPERIMENTAL

Test CMOS/SIMOX circuits with WSi_x/n+-poly gate were fabricated using our conventional process technologies on the assumption that any 0.35um CMOS devices should be fabricated only with less expensive simple process technologies [9], without using any novel gate materials, nor any elevated source and drain structures. In this case, the top silicon layer with an adequate thickness should be used to suppress the unfavorable increase in the source and drain parasitic resistance [3], and to control the transistor threshold voltage.Therefore, 120nm thick silicon layer was adopted in this study. The thicknesses of the buried oxide layer, the gate oxide film, and the LDD sidewall spacer were 400nm, 9nm, and 150nm, respectively. In order to fabricate different mode transistors, the impurity concentration in the transistor body (boron for NMOS, phosphorous for PMOS) was changed by different implant conditions. No metal-silicide was used for the source and drain regions.

3. RESULTS AND DISCUSSION

Fig. 1 shows the drain current of both NMOS and PMOS transistors as a function of the gate length for different body impurity concentration (transistor mode : PD, n-FD, and

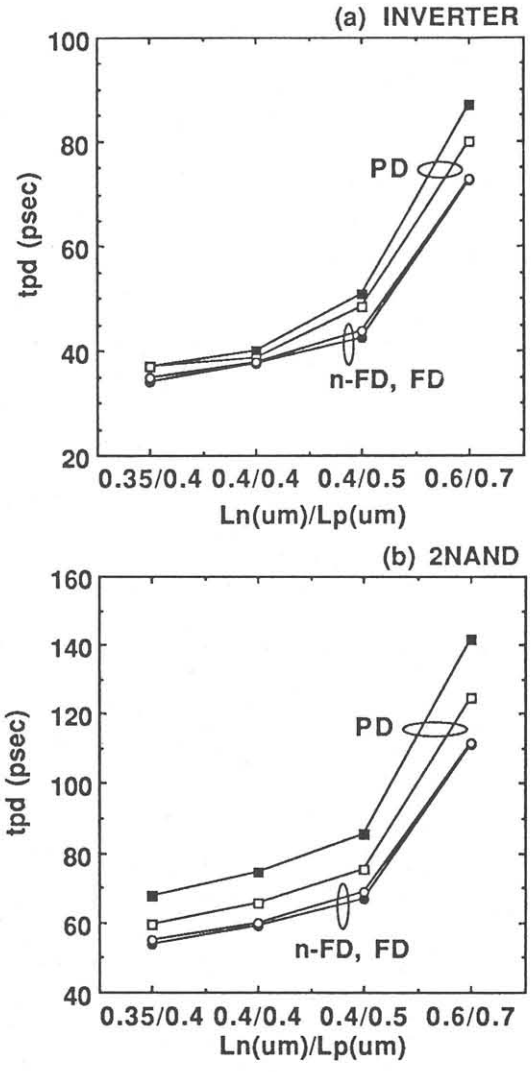


(Fig. 1) Drain Current of transistors as a function of the gate length for different impurity concentration in the transistor body. The substrate was grounded during the measurement.

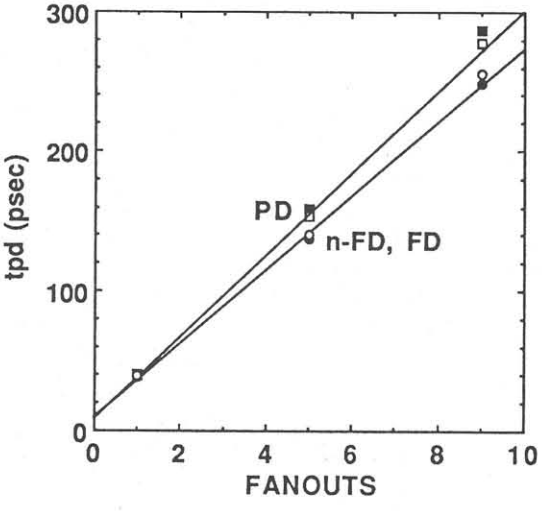
FD). As shown in this figure, the drain current increases with a decrease in the body impurity concentration for a given gate length. These results can be attributed mainly to a decrease in the threshold voltage as well as an increase in the channel mobility with a decrease in the impurity concentration. In order to suppress the short channel effects in both NMOS and PMOS transistors by a good margin for 0.35um devices, further studies on the transistor structures are required to determine the optimum combination of the thicknesses of the buried oxide layer and the top silicon layer, the LDD structure, and the body impurity profiles.

Fig. 2 shows the propagation delay time (tpd) of inverters and 2NAND gates composed of different mode transistors as a function of the gate length combination (Ln/Lp). The tpd decreases with a decrease in the body impurity concentration for a given gate length. For example, the tpd values for FD and PD mode inverters (Ln/Lp=0.35um/0.40um, V_{DD}=3.3V) are 34psec and 37psec, respectively. Since the value of the parasitic capacitance of each CMOS gate can be regarded as almost the same for any mode of transistors, these results can be attributed to an increase in the drain current of each transistor with a decrease in the transistor threshold voltage as a result of a decrease in the body impurity concentration. On the other hand, Fig. 2 also shows that the tpd differences among PD, n-FD, and FD mode inverters for a given gate length combination become smaller in the sub-halfmicron region, though it does not change so remarkably for 2NAND gates. Such difference between the inverter and the 2NAND gate can be attributed mainly to the difference in the discharge process of the parasitic capacitance which in turn depends strongly on the drain current of the NMOS transistor. It is known that the floating body effect causes a decrease in the threshold voltage in the PD mode NMOS transistors with an increase in the drain voltage, and/or with a decrease in the gate length, resulting in an increase in the drain current [8, 10]. Since the voltages of the source and the drain of each NMOS transistor connected in series in any NAND gates change dynamically, the body effect in the PD mode NMOS transistors does not affect the fall time of the pull down process so effectively, while it does strongly in the inverter. Therefore, if PD transistors have adequate body-contacts not to allow the floating body effect, the speed performance of PD mode inverters as well as NAND gates will become worse. Similar results (increases in the tpd) can be observed for PD cases in Fig. 4 at lower V_{DD} (<3.3V).

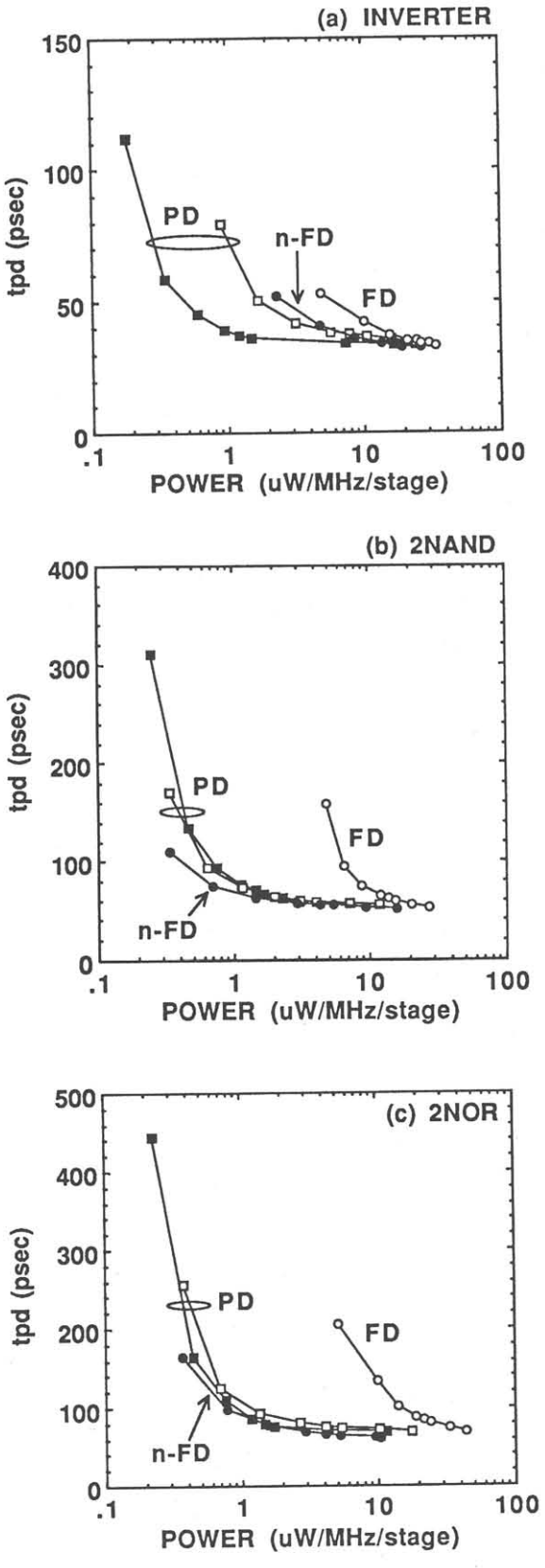
In order to investigate the reduction effect of the parasitic gate capacitance of the FD mode transistor in the subthreshold region ($[1/C_{gate}+1/C_{soi}+1/C_{box}]^{-1}$) on the tpd values, we measured the tpd dependence on the fan out number. Fig. 3 shows the results. Since the charge/discharge times ($V_{GS}>V_{th}$) are much longer than the transient time of the gate voltage in the subthreshold region ($V_{GS}<V_{th}$), we believe that the small difference in the line slope shown in Fig. 3 can be attributed mainly to the difference in the transistor drivabilities, and that the contribution of the reduced parasitic gate capacitance of the fully depleted mode transistor in the subthreshold region to the performance improvement is much smaller than expected.



(Fig. 2) Propagation delay times (tpd) of CMOS/SIMOX gates composed of different mode transistors as a function of the combination of the gate length (Ln/Lp). Wn/Wp=20um/20um, V_{DD}=3.3 volt, fanout=1.



(Fig. 3) Propagation delay times (tpd) of inverters composed of different mode transistors as a function of the fanout. Ln/Lp=0.4um/0.4um, Wn/Wp=20um/20um, V_{DD}=3.3 volt.



(Fig. 4) Propagation delay times (tpd) of CMOS/SIMOX gates composed of different mode transistors as a function of power consumption. Ln/Lp=0.35um/0.40um, Wn/Wp=20um/20um, fanout=1. Power supply voltages are 1.5, 2.0, 2.5, 3.0, 3.3, 3.5, 4.0, and 4.5 volt.

Fig. 4 shows the relationship between the tpd and the power consumption for different ring oscillators. For a given tpd (ex. 40psec), the power consumption of the inverter increases with a decrease in the body impurity concentration (from PD toward FD), though NAND and NOR gates showed slightly different trend. These results can be attributed to an increase in the overlap current due to a decrease in the threshold voltage of each transistor. It should be noted that only the V_{DD} does not necessarily determine the power consumption of CMOS/SIMOX circuits and that if the overlap current is too large, both the tpd and the power consumption cannot be reduced in spite of the reduced drain parasitic capacitance. Therefore, the design & control of the transistor threshold voltage is a significant issue to realize practical, high-speed, low-power CMOS/ SIMOX devices.

4. SUMMARY

In summary, we investigated the propagation delay time and the power consumption of several CMOS/SIMOX gates composed of different mode transistors, which were fabricated on the assumption that any 0.35um CMOS devices should be fabricated only with less expensive simple process technologies. On the basis of our experimental results, it is concluded that the reduced drain parasitic capacitance with SOI structures is the most essential factor for low-power, high-speed performances [4-9, 11], and that the design & control of the threshold voltage of each transistor is the most significant issue to realize low-power CMOS/SIMOX circuits. Outstanding advantages of fully depleted mode itself in circuit performances were not found in this study.

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