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Scaling Theory for V_{th} Controlled n^+-p^+ Double-Gate SOI MOSFETs

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We have established a scaling theory for n^+- p^+ double-gate SOI MOSFETs, which gives us the guidance to design devices with a sub 0.1-μm L_G. We also propose models for threshold voltage V_{th} and drain current I_D. Although the I_D model is for long-channel devices, numerical analysis shows that it is valid even for sub 0.1-μm-L_G devices that have been designed based on the scaling theory. According to our theory, we can design a sub 0.1-μm-L_G device with an ideal subthreshold swing (S-swing) and appropriate V_{th}.

I. Introduction

Double-gate SOI MOSFETs are expected to overcome the scaling limits of bulk MOSFETs. However, since the work function of the gate material determines V_{th}, we must investigate suitable gate materials to obtain a proper V_{th}[1]. To alleviate the hurdle, we proposed an n^+- p^+ double-gate SOI MOSFET in which V_{th} is controlled by the interaction between the front and back gates (Fig. 1). Furthermore, we demonstrated a CMOS inverter delay of 27 ps for a device with $L_G = 0.2$ μm and $t_{Ox} = 9$ nm at supply voltage V_{DD} of 2 V. This device had a V_{th} of 0.25 V with an ideal S-swing[2].

We have established a scaling theory for the device and revealed the potential of how short channel region can this device go.

II. Threshold Voltage

In both p^+- p^+ and n^+- p^+ double-gate SOI MOSFETs (Fig. 1), both gate oxide thicknesses t_{Ox} are the same, and the same gate voltage V_G is applied to the both gates. The channel doping concentration N_A is constant, independent of gate length L_G, and is as low as 10^{15} cm^{-3}.

Based on numerical analysis, we assumed a linear vertical potential distribution in the channel region, as shown in Fig. 2. To clarify the analysis, t_{Ox} is enlarged by γ which is $\varepsilon_{Ox}/\varepsilon_{Si}$, which enables us to express a potential distribution with a straight line in the entire gate oxide and channel regions.

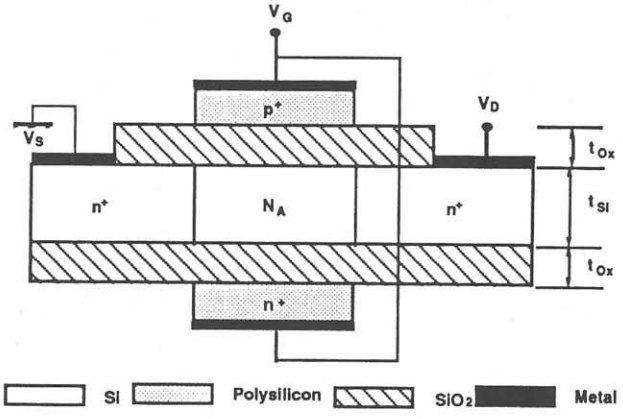

Fig. 1 n^+- p^+ double-gate SOI MOSFET.

For p^+- p^+ double-gate devices, the potential is constant in the entire channel region, and the transistor switches on when the potential reaches a certain value ϕ_{sth} given by

$$\phi_{sth} = V_{th}(p^+ - p^+) - V_{FBp^+}, \qquad (1)$$

where $V_{th}(p^+$- $p^+)$ is the threshold voltage of the p^+- p^+ double-gate device given in [1] and V_{FBp+} is the flatband voltage associated with the p^+ polysilicon.

The potential distribution of the n^+- p^+ double-gate devices has a gradient due to the difference between the flat band voltages at each gate ΔV_{FB} which is almost the band gap of Si. The potential shifted parallel maintaining its gradient with V_G, and the inversion layer is then formed on the inside surface of the n^+ polysilicon gate (the point D in Fig. 2). By using similar triangles for ABC and AED, we obtain

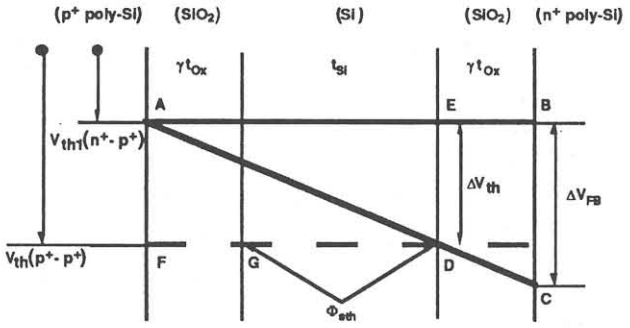

Fig. 2 Schematic potential distributions: a dashed line corresponds to a p^+- p^+ double-gate device and a solid line to a n^+- p^+ double-gate device.

$$V_{th1} = V_{th}\left(p^+ - p^+\right) - \frac{\gamma t_{Ox} + t_{Si}}{2\gamma t_{Ox} + t_{Si}} \Delta V_{FB} \quad . \qquad (2)$$

When V_G increases further, the line AD changes to become the line FD. When the point A reaches the point F, the inversion layer is formed on the inside surface of the p^+ polysilicon gate (the point G in Fig. 2). Therefore, the second threshold voltage associated with the p^+ polysilicon gate is

$$V_{th2} = V_{th}\left(p^+ - p^+\right) , \qquad (3)$$

which is the same as that of p^+- p^+ double-gate devices.

The numerical data agrees well with the analytical model (Fig. 3). $V_{th}(p^+$- $p^+)$ is about 1 V and threshold voltage of n^+- n^+ double-gate devices is - 0.1 V, both of which are inadequate for deep submicron gate length devices.

Since $V_{th}(p^+$- $p^+)$ and ΔV_{FB} in Eq. 2 are almost independent of t_{Ox} and t_{Si}, the magnitude of V_{th1} is a function of t_{Ox}/t_{Si}, and is about 0.25 V for $t_{Ox}/t_{Si} = 5$. V_{th2} is about 1 V independent of t_{Ox} and t_{Si}, and hence both channels contribute to current conduction when V_{DD} exceeds 1 V, but the p^+ polysilicon gate only controls V_{th1} when V_{DD} is less than 1 V.

III. Drain Current Model

We regarded the device as being two transistors connected in parallel with a different V_{th} for each gate. Applying a drain current model developed for bulk MOSFETs[3] to each gate, we proposed I_D model given by

$$I_D = \sum_{i=1,2} \frac{W\mu_{n\text{-}i}}{L_G\left[1 + \dfrac{\mu_{n\text{-}i}\left(\dfrac{V_D}{L_G}\right)}{2v_{ns}}\right]} \left[\left(V_G - V_{th\text{-}i}\right)V_D - \frac{1}{2}V_D^2\right] \quad . \qquad (4)$$

The validity of the model will be verified in the next section.

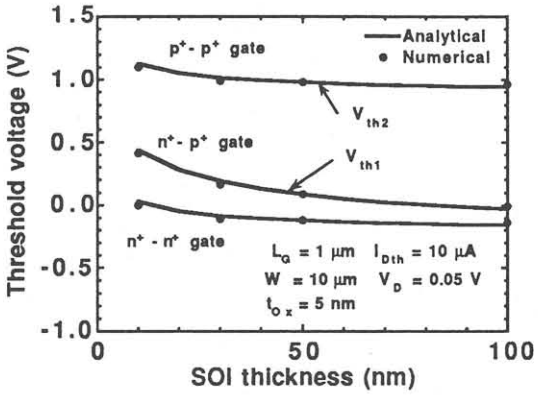

Fig. 3 Dependence of threshold voltage on SOI thickness.

V. Scaling Theory

We solved the two-dimensional potential distribution in the channel region by a method similar to that described in [4], we found that the minimum potential along the punch-through current path is a function of the natural length λ pertaining to n^+- p^+ and p^+- p^+ double-gate devices:

$$\lambda\left(n^+ - p^+\right) = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{Ox}} t_{Ox} t_{Si}}$$

$$\lambda\left(p^+ - p^+\right) = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{Oxi}} t_{Ox} t_{Si}\left(1 + \frac{\varepsilon_{Ox}\, t_{Si}}{4\varepsilon_{Si}\, t_{Ox}}\right)} \quad . \qquad (5)$$

Assuming that the minimum potential determines the S-swing, we obtained the following analytical S-swing expression:

$$S = \frac{\ln 10}{\beta} \frac{1}{1 - 2\exp\left(-\dfrac{L_G}{2\lambda}\right)} \quad . \qquad (6)$$

According to our theory, if $L_G/(2\lambda)$ is the same, the S-swing is the same for p^+- p^+ and n^+- p^+ double-gate devices. This means that the n^+- p^+ double-gate device suffers less from short-channel effects than the p^+- p^+ double-gate device because $\lambda(n^+$- $p^+)$ is always smaller than $\lambda(p^+$- $p^+)$. This can be qualitatively explained as follows: The punch-through current flows along the center of the SOI in p^+- p^+ double-gate devices, and at the surface in n^+- p^+ double-gate devices, and the potential is controlled more strongly at the surface.

The analytical model agrees well with the experimental and numerical data (Fig. 4). Our results show that we should design the device so that $L_G/(2\lambda)$ is more than 3.

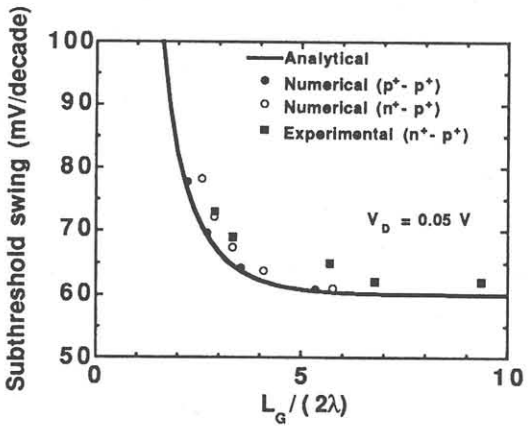

Fig. 4 Dependence of subthreshold swing on $L_G/(2\lambda)$. Device parameters used in numerical calculation: t_{Ox} = 5 nm, L_G = 0.1 μm, and various t_{Si}. Experimental device parameters: t_{Ox} = 9 nm, t_{Si} = 40 nm, and various L_G.

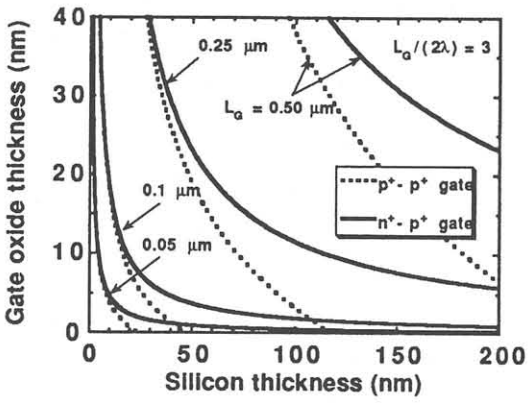

Fig. 5 Relationship between SOI and gate oxide thicknesses for various gate lengths.

Once $L_G/(2\lambda)$ is determined (we chose a value of 3), the relationship between t_{Ox} and t_{Si} is obtained directly (Fig. 5). The t_{Ox} and t_{Si} values for a given L_G should be selected in the lower region of the corresponding L_G curve. The allowable region decreases with decreasing L_G and is wider for n^+- p^+ double-gate devices than for p^+- p^+ double-gate devices.

Consider the device with a L_G of 0.1 μm. t_{Ox} of this device is expected to be 3 nm [5], and we set t_{Si} to 15 nm to obtain an appropriate V_{th}. This (t_{Ox}, t_{Si}) point is in the allowable region in Fig. 5. Using the same mobility model, we compared the analytical I_D model with the numerical data (Fig.6). Since the analytical model neglects short channel effects, the good agreement means that we can regard devices designed adhering the scaling theory as long-channel devices even for L_G = 0.1 μm.

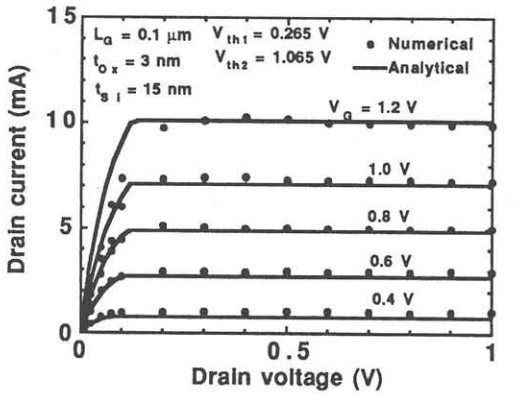

Fig. 6 Comparison between numerical and analytical current-voltage characteristics.

IV. Conclusion

n^+- p^+ double-gate SOI MOSFETs suffer less from short-channel effects than p^+- p^+ double-gate SOI MOSFETs. Using these devices, we can overcome the scaling limits of bulk MOSFETs and design devices with L_G of less than 0.1 μm, while maintaining an ideal S-swing and proper V_{th}.

Acknowledgment

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