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Some Properties of SOI Gate-All-Around Devices

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Gate-All-Around transistors have been studied from the point of view of radiation hardness and their electrical characteristics have been measured at low temperature. It is found that GAA devices can withstand high doses of gamma ray radiation with relatively small threshold voltage shifts and no edge leakage current. When the device is operated at low temperature, transconductance peaks due to two-dimensional carrier confinement are observed. This confinement effect has been modeled using a self-consistent Poisson-Schrödinger solver.

1. INTRODUCTION

Gate-all-Around (GAA) devices are SOI thin-film (t_{si} <100 nm) devices where the gate electrode covers both the top and the bottom of the device. The fabrication process is described in ref. 1. Cross-sections of the transistor are presented in Fig.1. The P-type channel doping of the N- and P-channel transistors is 10^{17} and $5x10^{16}$ cm^{-3}, respectively.

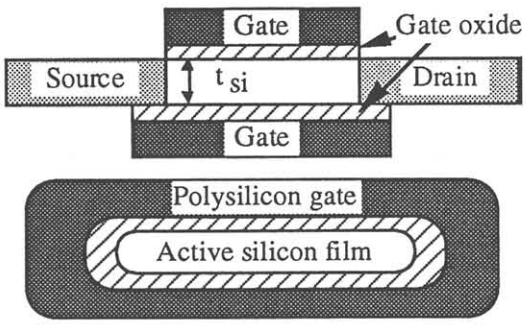

Fig. 1: GAA device cross-sections: parallel (top) and perpendicular (bottom) to current flow direction.

2. RADIATION HARDNESS

The degradation of a MOSFET caused by gamma or X-ray irradiation is mainly due to charge generation and trapping in the oxides and to interface state generation. The thicker the oxide, the more charges are generated. In the GAA device, the active region is completely surrounded by thin, high-quality gate oxide. Since no field oxide is in contact with the channel region, irradiation-induced edge leakage current can be eliminated[2]. The following results concerns 3x3μm N- and P-channel transistors mounted in an inverter configuration during irradiation. Their common gate was continuously switched between 0V and 3V at the low frequency 200Hz. The devices were irradiated using a ^{60}Co gamma source with a dose rate of 4.2rad(Si)/sec below 2.2Mrad(Si) and 13.2rad(Si)/sec up to 18Mrad(Si). Measurements were performed *in situ* to avoid partial recovery.

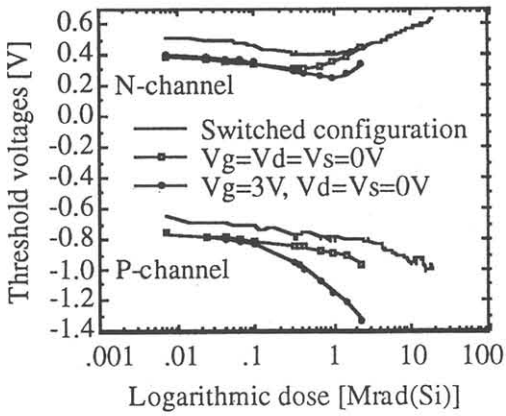

Fig. 2: Threshold voltage evolutions *vs.* total dose.

Fig. 2 presents the evolution of both threshold voltages, V_{tn} and V_{tp}, as a function of irradiation dose. Although the gate oxide is not very thin (30 nm), the radiation hardness proves to be quite good. V_{tn} decreases from 0.51V to 0.40V around 350krad(Si) and then rebounds to 0.62V at 18Mrad(Si). V_{tp} steadily drops from -0.65V to -0.88V. Other dc bias configurations are presented as well. The maximum transconductances of N- and P-channel transistors decrease by the same amount (20% after 18Mrad(Si)) so that their ratio remains perfectly constant. The leakage current is negligible in P-channel, less than 10^{-10} A (lowest measurable current in our experimental set-up)

and reaches a maximum value of 20nA, at the dose giving minimum V_{tn}, in 3×3µm N-channel devices with the drain-to-source voltage V_{ds}= 50mV (Fig. 3).

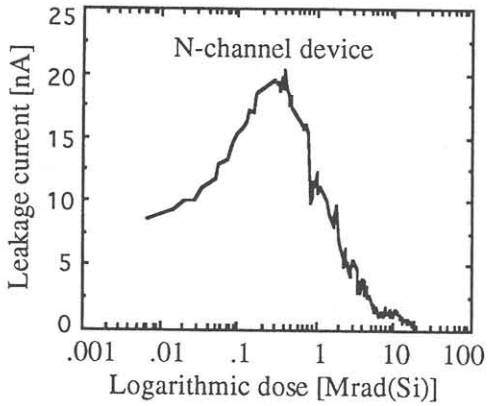

Fig. 3: Leakage current of 3×3µm N-channel devices *vs.* total dose, with V_{ds}=50mV.

Memories containing few cells (64) but with highly variable transistor sizes were realized in order to verify how far the GAA technology could withstand total dose, even with very sensitive designs. We have chosen a six-transistor cell design with N-channel pass devices. The load transistor size $(w/l)_P$ of the flip-flops are spread around the value that gives a symmetrical transfer characteristic of the inverters. It is possible to numerically prove that cells with small $(w/l)_P$ have an access device size much greater than the minimum required by the write operation. This particular design emphasizes the sensitivity to mismatch between the precharge levels and enhances the mutual interaction between cells through leakage currents, like in very dense memories. On the other hand, cells with a greater $(w/l)_P$ are close to the minimum access transistor size and investigate the robustness of the write operation. A checkerboard algorithm was used during irradiation. If necessary, the time of occurence and the location of the errors were recorded by an HP16500 logic analyzer coupled to a PC but not a single error occured.

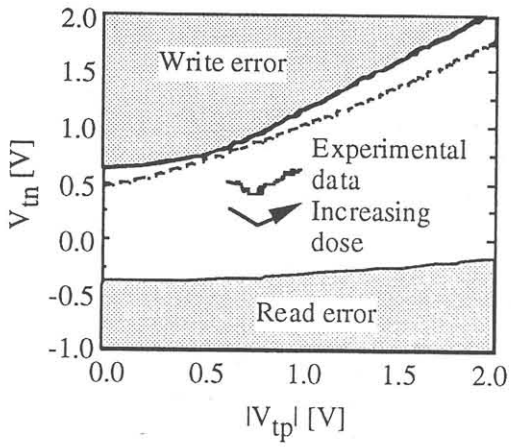

Fig. 4: Limits of the read and write operations, and the path followed in the V_{tn}-V_{tp} plane during irradiation.

Fig. 4 presents the tightest limits, computed numerically, of the write and read operations together with the path followed in the V_{tn}-V_{tp} plane during irradiation. The threshold voltage shifts are so modest that the operating point stays far from the write and leakage failures. Although the memories were very sensitive to discrepancies between the precharge levels, the read operation was not affected. The continuous switching of the cells unfortunately prevented the analysis of the so-called "imprinting" effects. Nevertheless, the write boundary seems not beeing strongly degraded when imprinting occurs (dotted curve). Therefore these first experimental results tend to prove the robustness of the GAA technology at least up to 18Mrad(Si).

3. TWO-DIMENSIONAL EFFECTS

Right above threshold, the N-channel GAA device behaves as a two-dimensional electron gas (volume inversion effect[3]). In such a case, the conduction band splits in a series of subbands, and 2D quantum effects are observed. In a first approximation, the simple "particle in a box" approach can be used to estimate the values of the minimum energy of the subbands. These values are given by the following expression:

$$E_{n-1} = \frac{\hbar^2}{2m^*}\left(\frac{\pi n}{t_{si}}\right)^2$$

where m^* is either the lateral or the transverse effective mass.

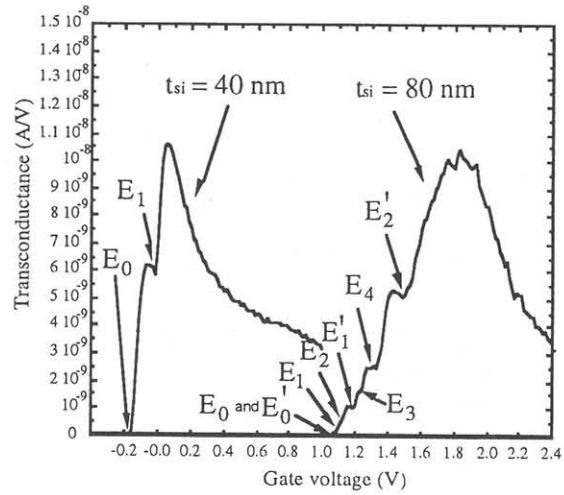

Fig. 5: Transconductance *vs.* gate voltage for two silicon film thicknesses. The energy levels corresponding to TPVs are indicated.

Fig. 5 presents the measured transonductance of 40 nm- and 80 nm-thick N-channel GAA devices as a function of gate voltage (T=300 mK, V_{ds}=30mV). The different transconductance peaks and valleys (TPVs) correspond to the population of different subbands (E_0 corresponds to the first subband ($m^*=m_l$), E_1 corresponds to the second subband ($m^*=m_l$), E'_0 corresponds to the first subband with $m^*=m_t$, etc...). Classical effective masses in silicon are used (m_l=0.98

m_0 and m_t=0.19 m_0). The relationship between gate voltage and surface potential can be approximated using a classical (non-quantum mechanical) device simulator[4].

A more exact approximation can be obtained by solving the Poisson and Schrödinger equations self-consistently. The general evolution of the energy levels and the wave functions is presented in Fig. 6, for a single effective mass value. If the depletion and inversion charges are low enough (undoped device right above threshold), the potential well into which the electrons are confined can be considered as square. The position of the energy levels are then given by the equation above and the normalized wave functions are given by $\Psi(x)=\sin(n\pi x/t_{si})$, where t_{si} is the silicon film thickness. When the inversion charge in the film increases (right above threshold), the potential well becomes parabolic and the electrons become more attracted by the gates. The energy levels shift upwards and tend to pair up (E_0 pairs with E_1, E_2 with E_3, etc...). Finally, for higher gate voltages, the energy levels become degenerate through pairing, and the wave functions are located mostly at the interfaces, close to the gate oxides (formation of inversion channels). The transconductance peaks are observed for the "square well" and "weak parabolic well" situations, where true volume inversion is present.

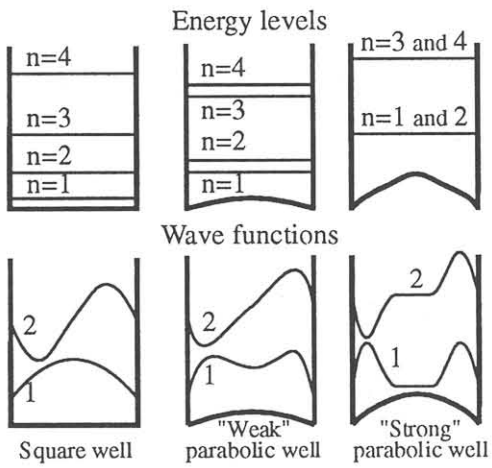

Fig. 6: Four first energy levels and two first wave functions in square, weak parabolic and strong parabolic potential wells.

Fig. 7 presents the evolution of the electron concentration in the 40 nm-thick device as a function of gate voltage. One can clearly see the volume inversion right above threshold and the formation of two inversion channels at higher gate voltages.

Fig. 8 presents the evolution of the subband energy levels as a function of gate voltage. The plot is realized in such a way that the Fermi level remains constant. Every time an energy level falls below the Fermi level, the corresponding subband becomes populated.

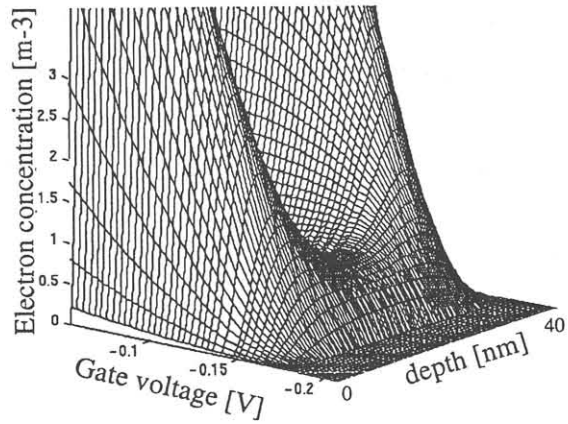

Fig. 7: Electron concentration *vs.* depth in the silicon film and *vs.* gate voltage (40 nm device).

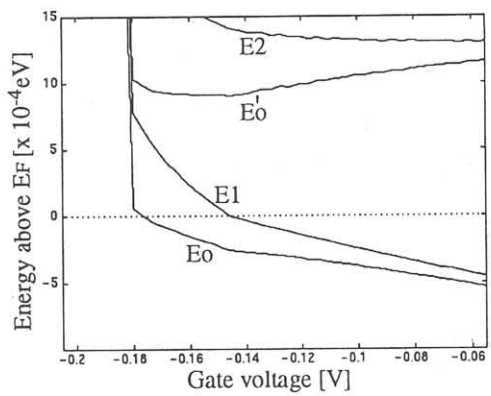

Fig. 8: Evolution of energy levels (relative to E_F=0) as a function of gate voltage (40 nm device).

4. CONCLUSION

We have shown that GAA devices and small memories can withstand high total dose of gamma ray radiation. Threshold voltage shifts are found to be relatively small and no edge current appears. Electrical characteristics of GAA transistors have also been measured at low temperature showing transconductance peaks due to two-dimensional carrier confinement. This 2D quantum effect is satisfactorily modeled using a self-consistent Poisson-Schrödinger solver.

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REFERENCES

1) J.P. Colinge, M.H. Gao, A. Romano, H. Maes and C. Claeys, Proceedings IEDM (1990) 595.
2) J.P. Colinge and A. Terao, IEEE Trans. Nuclear Science NS-40 (1993) 78.
3) F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa, IEEE Electron Device Letters EDL-8 (1987) 410.
4) J.P. Colinge, X. Baie and V. Bayot, IEEE Electron Device Letters to be published June 1994.