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Nanometer Scale MOSFETs and STM Patterning on Si

J. R. Tucker, C. Wang, J. W. Lyding, T.-C. Shen, and G. C. Abeln

Depatment of Electrical and Computer Engineering and Beckman Institute
University of Illinois, Urbana, IL 61801 USA

A scanning tunneling microscope (STM) has been used to selectively desorb hydrogen from UHV H-passivated Si(100)-2x1 surfaces with ~1nm resolution. Oxidation of the depassivated areas within a load-lock at room temperature and ~1atm O_2 pressure preserves the pattern resolution. A new theoretical principle for ultra-small MOSFETs has also been proposed, based on gate-induced tunneling through a Schottky barrier located at the interface between a silicide source and the Si channel. Simulations indicate extraordinary possibilities if this principle can be experimentally demonstrated.

I. STM Lithography Experiments

A variety of approaches to STM-induced surface modification have recently been proposed. The highest resolution has been achieved with atomic manipulation techniques in UHV, as exemplified by the work of Lyo and Avouris[1] and Aono, et al.[2] on adatom extraction from Si surfaces. These methods depend upon strong atomic interaction between tip and substrate, and stability is therefore difficult to achieve. We have chosen a less perturbative approach, based upon previous ambient experiments by Dagata, et al.[3], which represents perhaps the ultimate extrapolation of conventional e-beam lithography. In our experiments, the STM's highly-confined electron beam is used in field emission to locally desorb a monolayer of hydrogen from UHV-passivated Si(100)-2x1:H surfaces. Our long-term goal is to combine STM lithography with *in situ* etching and metalization techniques in order to fabricate experimental device structures on the smallest possible scale.

Experiments[4] were performed on B-doped samples (0.1Ωcm) heated to 1250°C in UHV for one minute to produce a clean Si(100)-2x1 surface. Atomic hydrogen dosing was then carried out by cracking molecular H_2 on a 1500°C tungsten filament placed 6cm from the surface of a sample heated resistively to 650K. The chamber was back filled with 10^{-6} Torr of H_2 and total exposures of 400-1200L ensured a uniform saturated coverage of the monohydride. Dc-etched tungsten STM probes had 30-150Å radii of curvature, as verified by TEM imaging. STM depassivation is carried out by ramping the probe voltage into low field emission, with $-V_t>4V$, under feedback control. Subsequent imaging at –2V tip bias and 0.1nA clearly reveals the pattern. All transitions between patterning and normal scanning conditions are made smoothly, yielding highly reproducible results while preventing degradation

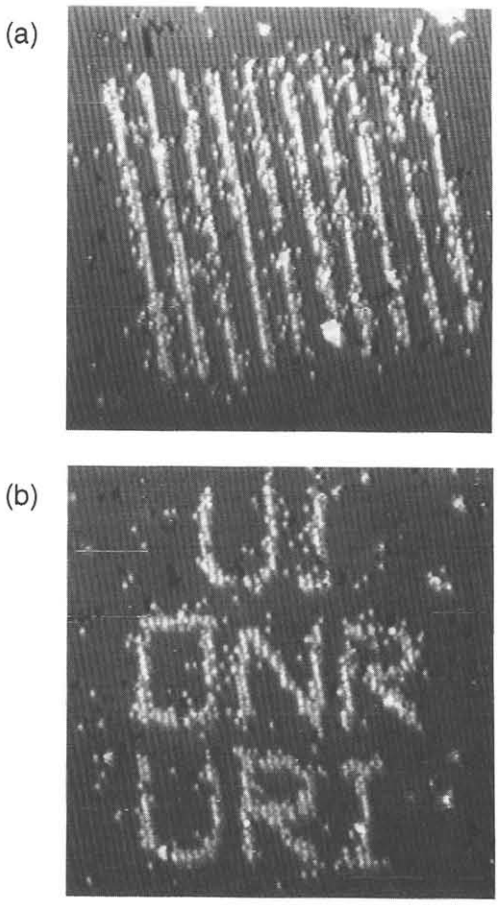

Fig.1 (a) STM depassivated lines written 30Å apart on Si(100)-2x1:H in UHV at –4.5V tip bias, 2.0nA, and $2x10^{-3}$C/cm line dose. (b) The letters UI ONR URI. Both images are 400Åx400Å.

of the tunneling probe.

Figure 1 shows a series of ~15Å wide parallel lines spaced 30Å apart, written at –4.5V and 2nA using a line dose of $2x10^{-3}$C/cm. This extremely high line dosage compared to conventional e-beam lithography is easily accessible with STM, and typical writing speeds are 0.01–1μm/s. Depassivation is only observed for negative tip bias, and larger voltages increase the linewidth due to increased tip-sample spacing. Patterning is very stable and reproducible once good resolution is achieved, since the probe tip does not interact directly with the sample. The detailed mechanism of hydrogen desorption is currently under study, and may be similar to the local heating picture suggested by Walkup, Newns, and Avouris[5] based on the dipole interaction between tunneling electrons and Si-bonded hydrogen.

Local restoration of the clean Si(100)-2x1 surface is confirmed by detailed STM spectroscopy and suggests numerous possibilities that are now only beginning to be explored. Room temperature oxidation of the exposed regions at ~1atm O_2 pressure within the system load-lock preserves both the remaining hydrogen passivation and the pattern linewidth. Further experiments on selective chemistry and pattern transfer are currently underway.

II. Tunneling MOSFET Simulations

Looking well into the future, we have given some thought to the types of devices which might benefit from the ability to pattern Si and related materials on the nanometer scale. One idea[6] is to utilize the gate-induced band-bending within a MOSFET structure to regulate tunneling of carriers through a Schottky barrier formed at the interface between a silicide source electrode and the semiconductor channel. An idealized self-aligned structure is sketched in Fig. 2, with source S and drain D composed of metal silicide coplanar with the Si channel. When a gate voltage is applied across the ultra-thin insulator of thickness d~40Å, large electric fields will be induced near the top corners of the source and drain. The resulting band-bending can be sufficient to generate extremely large tunnel current densities at the source, as carriers penetrate the Schottky barrier by internal field emission (Fowler-Nordheim tunneling). The presence of a source Schottky barrier greatly reduces short-channel effects, so that gate lengths can be substantially reduced. At room temperature, some doping of the semiconductor channel region will be required in order to suppress thermionic emission currents over the barrier. At 77K, however, no impurity doping of the channel is needed, since the Schottky barrier itself will then be sufficient to confine the carriers. In this case, ground planes can be tailored to optimize interconnect performance, and isolation between devices can be entirely eliminated.

It appears that a device of this type could be fabricated by employing a variant of the standard salicide process, as sketched in Fig. 3. Here an ultra-thin SiO_2 sidewall spacer with thickness ~50-100Å is first used as a mask for Cl RIE, in order to etch source and drain wells into the Si substrate. A metal film (in this case Pt) is then evaporated and sintered to form silicide within these source and drain regions and also on top of the polysilicon gate, using the sidewall spacer to isolate the gate as in the standard salicide process. The key step here is to insure that lateral diffusion of metal atoms exceeds the spacer thickness, in order to establish gate overlap at source and drain. Simulations indicate that output characteristics are insensitive to the amount of gate overlap, but any open gap between the gate and source could make it impossible to turn the device on. The noble and near-noble metals Pt, Pd, Co, and Ni are preferred in this application because the metal atom is the primary diffuser in thermal formation of the silicide (unlike the refractory metal silicides of Ta, Ti, Mo, and W).

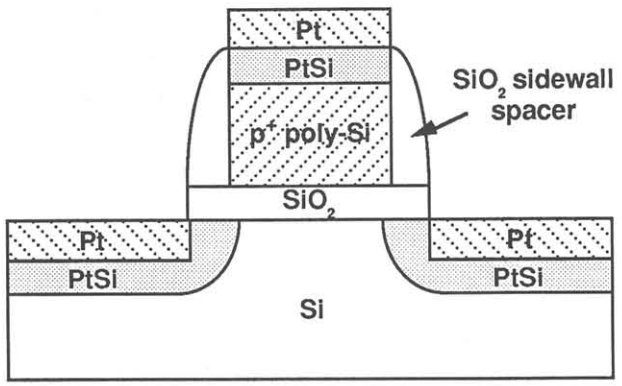

Fig.3 Use of a very thin SiO_2 sidewall spacer in fabrication of silicide source and drain wells coplanar with Si channel. Gate overlap is established by lateral diffusion of metal atoms underneath the spacer during silicide formation.

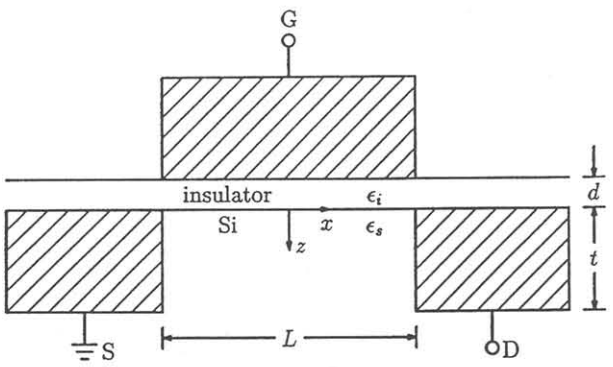

Fig.2 Tunneling MOSFET structure with silicide source and drain electrodes coplanar with the Si channel.

Computed output characteristics are shown in Fig. 4 for a p-channel device at 77K with gate length L=500Å, oxide thickness d=30Å, and Schottky barrier height Φ_B=0.25eV between its PtSi source and drain electrodes and the Si channel. In this case, a negative applied gate voltage induces tunneling of light holes, effective mass $m_{lh}^*=0.16m_0$, out of the source and into the channel. The substrate is undoped, and gate voltages are expressed relative to the flat-band voltage, here simply the difference in work function between source and gate. For a p^+ polysilicon gate $V_{FB}\approx\Phi_B$=+0.25V, so that the magnitude of the applied gate voltages would be reduced by this amount. The device shown in Fig. 4 could thus be operated at a supply voltage $V_S\approx$1.2V with maximum drain current $I_D^{max}\approx$1.5A/cm and leakage current $I_D^{min}\approx10^{-7}$A/cm. Increasing the gate length to L=600Å reduces the leakage by an order of magnitude, to $I_D^{min}\sim10^{-8}$A/cm (1pA/μm).

Use of $Si_{1-x}Ge_x$ channels could further reduce electric fields and supply voltages. The light hole mass in pure Ge, $m_{lh}^*\approx0.04m_0$, is smaller by a factor of ~4 than in Si, for example. Lower Schottky barriers $\Phi_B\sim$0.15eV could also be utilized at 77K. Either of these possibilities would lower the electric field scale in the semiconductor by a factor ~2 according to the Fowler-Nordheim expression. Si_3N_4 or even CaF_2 could then be employed as the gate insulator, resulting in further reductions of ~2 in supply voltage due to their higher dielectric constants. Use of lattice-matched silicides in combination with CaF_2 and other epitaxial insulators might eventually provide a route to 3-dimensional integration.

The following list summarizes several potential advantages of this approach:
(1) Minimum gate lengths L~400-500Å.
(2) Minimum supply voltages $V_s\sim$1.0V at 300K and $V_s\sim$0.5V or less at 77K.
(3) Contact areas are greatly reduced with silicide source and drain electrodes.
(4) Isolation requirements are minimized or eliminated.
(5) Absence of impurities in the semiconductor channel implies higher thermal budget.
(6) Simplified structure facilitates fabrication at ultra-small dimensions.
(7) Potential for epitaxial insulators and silicides is consistent with future 3-dimensional architectures.

An experimental demonstration of field-effect control of tunneling in MOSFET structures might thus open extraordinary new possibilities for high density and low power integrated circuits.

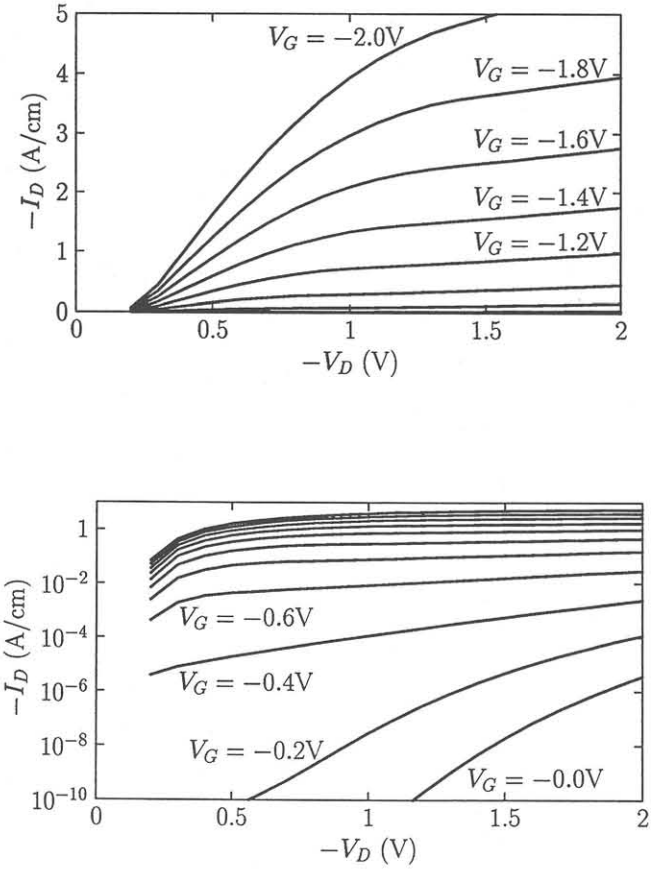

Fig.4 Output characteristics computed for a p-channel tunneling MOSFET with gate length L=500Å, oxide thickness d=30Å, and Schottky barrier height Φ_B=0.25eV. Gate voltages are relative to flat-band.

Acknowledgements

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