Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 325-327

Invited

Room-Temperature Single-Electron Devices

Kazuo Yano, Tomoyuki Ishii, Takashi Hashimoto, Takashi Kobayashi,
Fumio Murai, and Koichi Seki

Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, Japan

This paper presents room-temperature operation, for the first time, of a single-electron memory element and a single-electron transistor. This is made possible by utilizing a quantum wire and quantum dot formed naturally in 3.4-nm ultra-thin poly-Si film. The fabricated ultra-thin-film transistors show a clear Coulomb staircase, evidence supporting room-temperature operation of a single-electron transistor, when the gate voltage is near the threshold voltage. When the gate voltage is varied over a larger voltage range, it shows quantized threshold shifts and memory effects. Single-electron memory offers the potential for fast, non-volatile ULSI memories, which goes far beyond conventional memory devices.

1. INTRODUCTION

Single-electron devices have recently attracted much attention because they show new physical phenomena in microstructures and provide the possibility for ultimate low-power devices. The operation of a single-electron transistor [1], single-electron turnstile [2], and single-electron memory [3,4] have been experimentally demonstrated. However, there is a major obstacle: single-electron devices, so far, work only at very low temperatures. In principle, room-temperature operation is possible with nanometer-scale structures [9], even though the nanometer scale is one order of magnitude smaller than the present limits of lithography resolution. However, there have been some encouraging observations. The current through an STM tip above a small metal particle is shown to be strongly affected by single-electron charging even at room temperature [6], and the random telegraph noises observed at room temperature [7] can be regarded as a single-electron phenomenon. However, it is believed that the time at which a single-electron device can function properly at room-temperature is still a long way off.

We tried to overcome this difficulty by combining natural nanostructures with state-of-the-art microfabrication techniques. In this way we came upon the idea of the ultra-thin poly-Si transistor. It facilitates room temperature operation as a single-electron memory [7] and a single-electron transistor [8]. This opens the door to *single-electron engineering*, an entirely new way of controlling the electrons in ULSI devices.

2. SINGLE-ELECTRON MEMORY

Principle and Conditions The key idea to enabling room-temperature memory operation is the novel one-transistor memory cell (Fig. 1 inset), which has very high charge sensitivity. In contrast, conventional single-electron memory consists of three devices [3]. The new cell has a floating-dot structure, which is similar to flash memories. However, to detect a single electron in a quantum dot, the following new condition must be satisfied [7].

$q/C_{gc}>kT/q$ (Readout condition),

where C_{gc} is the gate-channel capacitance. C_{gc} of less than 2 aF is required to achieve room-temperature operation. Another important condition is the ability to precisely control the number of electrons:

$q^2/(2C_{tt})>kT$ (Coulomb-blockade condition),

where C_{tt} is the total capacitance related to the storage dot. The third condition for memory operation is bistability for states "1" and "0":

$V_{bi}+V_{be}>q/C_{tt}$ (Bistability condition),

where V_{bi} and V_{be} are the effective barrier height between the reservoir and the storage dot when an electron is injected and ejected, respectively. The barrier should be higher than the voltage change caused by the Coulomb blockade.

Experiment The fabricated memory consists of an ultra-thin channel poly-silicon wire (3.4-nm thick and 100-nm wide) and a gate wire (8-nm thick and 100-nm wide) which crosses underneath the channel (Fig. 1). The gate oxide is 150-nm thick. The channel poly-Si is deposited as a-Si and crystalized at 750°C. SEM and TEM observations reveal that the film consists of silicon grains, each about 10-nm across (Fig. 1 inset, and Fig. 5).

We observed the following single-electron memory operations. When the gate voltage is less than V_{th}+5V (V_{th} is the threshold voltage) the fabricated transistor works as a field-effect transistor

(with some conductance modulations, as shown later). However, when the gate voltage exceeds V_{th}+10V (write operation), the transistor changes into a more resistive state, i. e., high-threshold state. This change is discrete and a quantization of threshold voltage is observed, as shown in Figs. 2 and 3. If the gate voltage is then set far below the threshold (erase operation), the transistor-state returns to the original low-threshold state. This hysteresis effect is very stable and expected to last about a year, is used as a memory element. If the gate voltage is set and held far above the threshold voltage, a stepwise reduction in current is observed (Fig. 4, left). All these discrete changes in current are features of the single-electron memory.

Grand-Canyon Model To explain the above behaviors, the following model is proposed. From TEM images (Fig. 5), it is clear that the poly-Si thickness is fluctuating around the average value from one site to another (roughly ±2 nm). Because of this, electron kinetic energy in the vertical direction dramatically changes from one site to another and acts as the potential energy for horizontal electron motion. For example, about a 300-meV energy difference arises between one site with 3.4-nm-thick Si and another site that is 1.7-nm thick. Our simulation of the potential landscape based on the real statistical thickness variations (Fig. 6) shows that a narrow current path (~10-nm wide) and small storage dots (~10-nm across) are formed naturally. The 10-nm spatial correlation in potential arises from the fact that the thickness is strongly related to the grain size.

By applying high gate voltage, one electron is trapped in a storage dot, which changes the conductance of the current path due to Coulomb repulsion. This explains the memory operation. This model predicts that the threshold shift ΔV_{th} relating to one-electron trapping is given by q/C_{gc} and the gate voltage required to add one electron into the storage dot ΔV_w is given by q/C_{gt} (C_{gc} is the capacitance between the gate and the bottleneck region in the current flow, and C_{gt} is the capacitance between the gate and the storage dot). Our 3-D capacitance simulation shows that C_{gc} and C_{gt} are 2 x 10^{-20}F. This corresponds to a ΔV_{th} and ΔV_w of 8 V, which agrees with our experimental observations.

Advantages Single-electron memory has the potential to break the limitations of conventional memory devices in many aspects. The simple one-transistor cell structure is suitable for high density storage. Because the write/erase operations are done by injecting/ejecting one electron, the endurance against write/erase cycles and the write/erase speed can be dramatically improved as compared to flash memories. Based on these features, the single-electron memory is considered to be an ideal memory device, combining the advantages of both DRAM and flash: making it fast and non-volatile.

3. SINGLE-ELECTRON TRANSISTOR

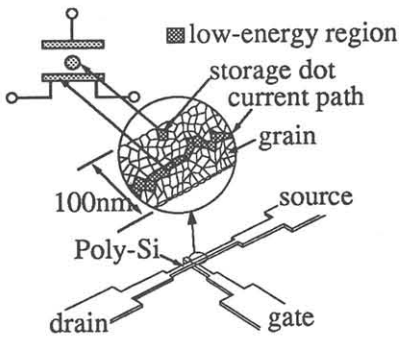
When the gate voltage is slightly lower than the threshold voltage, the current channel is delimited by some high barrier regions and an isolated dot is expected to be formed. This is confirmed by the observation of a clear Coulomb staircase in the device (Fig. 7). This is the first time known report of room-temperature operation by a single-electron transistor. The period of the staircase is given by q/C_{md} and the blurriness of the step is given by $2(kT/q)/(q/C_{mm})$, where C_{mm} is the total capacitance of the charging dot and C_{md} is the capacitance of the bottleneck junction between the charging dot and the drain. From the measured characteristics, we can estimate C_{mm} to be 2.1 aF, and C_{md} to be 1.4 aF. This again supports the proposition that charging is occurring in a 10-nm silicon grain.

4. CONCLUSIONS

We have demonstrated the first room-temperature operation of both single-electron memory and a single-electron transistor. This is made possible by utilizing the ultra-thin poly-Si natural nanostructures. The door is now open to room-temperature single-electron engineering, which will revolutionize the concept of ULSI device design. Better control of the structures is the next challenge to be faced in advancing this study.

Acknowledgement The authors would like to thank Dr. K. Nakazato, Dr. J. White, Dr. B. Alphenaar, Dr. D. Williams, Dr. J. Allam, and Dr. R. J. Blaikie of the Hitachi Cambridge Laboratory, Professor H. Ahmed of the Microelectronics Research Centre, Cambridge University, Professor D. K. Ferry of Arizona State University, Professor S. Katsumoto, and Dr. M. Ueda of the University of Tokyo, Dr. K. Shimohigashi, Dr. E. Takeda, Dr. M. Miyao, Dr. T. Shimada, Mr. H. Matsuoka, Mr. T. Yamanaka, Mr. S. Tachibana, and Dr. M. Aoki of the Hitachi Central Research Laboratory for their valuable discussions. The authors are also indebted to Dr. T. Nishida, Dr. S. Ohkura, Dr. T. Kure, and Mr. S. Iijima of the ULSI Research Center for device fabrication.

[1] T. A. Fulton, and G. J. Dolan, Phys. Rev. Lett. (1987).
[2] L. J. Geerligs, V. F. Andregg, P. A. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64**, 2691 (1990).
[3] K. Nakazato, R. J. Blaikie, J. R. Cleaver, and H. Ahmed, Electronics Letters, **29** (4), 384 (1993)
[4] P. D. Dresselhaus, L. J. Siyuan Han, J. E. Lukens, and K. K. Likharev, Phys. Rev. Lett. **72**, 3226 (1994).
[5] C. Schönenberger and H. van Houten, 1992 International Conference on Solid State Devices and Materials, 726 (1992).
[6] M. J. Kirton and M. J. Uren, Advances in Physics, **38**, 367 (1989).
[7] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE International Electron Devices Meeting 1993, 541 (1993); IEEE Trans. Electron Devices, Sept (1994).
[8] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, Hitachi Central Research Laboratory Workshop on "Physics and Applications of Single-Electron Phenomena," June (1994).
[9] For review, see for example, D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, Elsevier (1991); or H. Grabert and M. H. Devoret, eds., *Single-Charge Tunneling*, NATO ASI Series B (Plenum, New York, 1991).



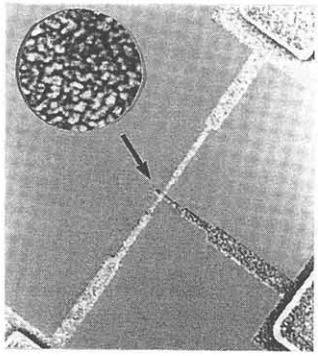


Fig. 1 Fabricated structure and an SEM photograph. The inset is the enlarged view of the active region, where the channel poly-Si and the gate cross.

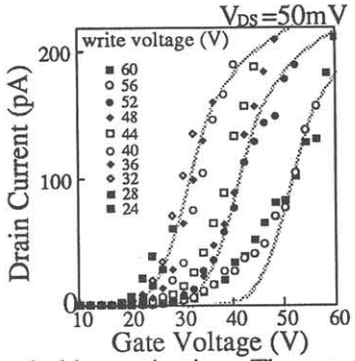


Fig. 2 Threshold quantization. The gate voltage is swept down from various write voltages.

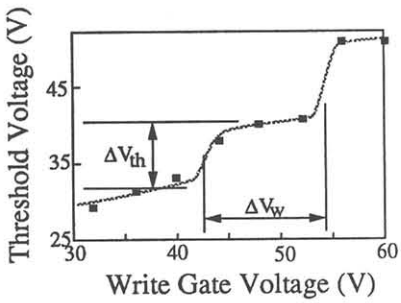


Fig. 3 The dependence of threshold voltage on write voltage.

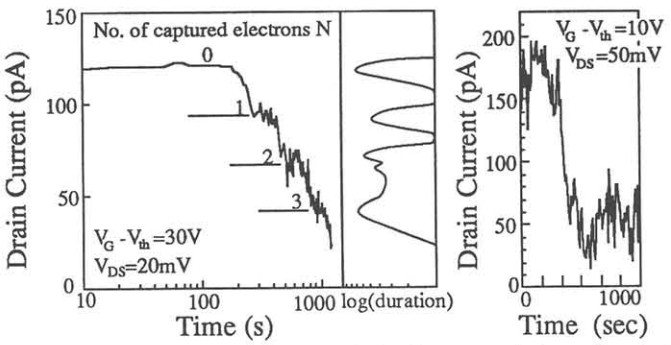


Fig.4 Temporal staircase and the integrated time for each current level (left). A giant leap is sometimes observed when Vg-Vth is smaller than the case shown on the left (right).

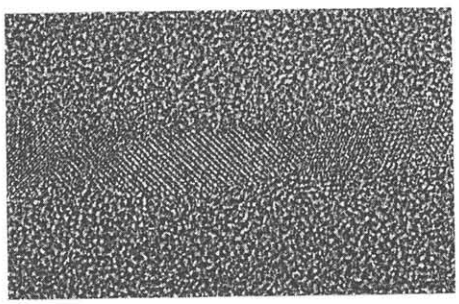


Fig. 5 Cross-sectional TEM photograph of the ultra-thin poly-Si.

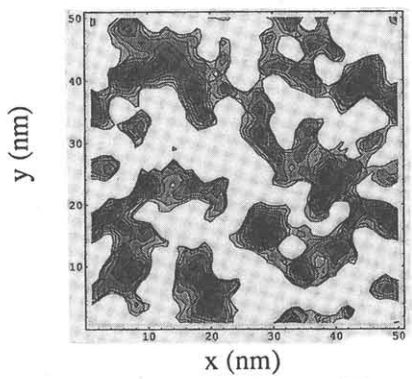


Fig. 6 Simulated potential landscape: "Nanometer Grand Canyon." The portion of the mountains above the 0.16-eV level (blank region) is removed to give a clear view of the canyons. Adjacent contour lines have a 16-meV energy difference.

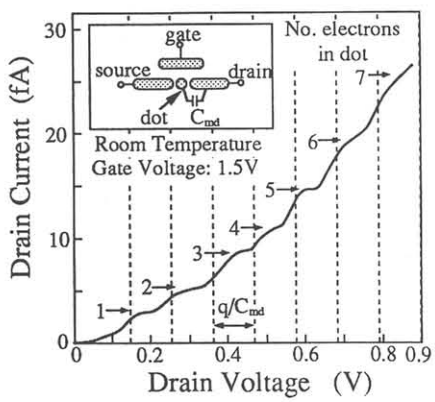


Fig. 7 A Coulomb staircase is evident when gate voltage is set slightly lower than the threshold voltage.