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Monte Carlo Study of Single-Electronic Devices

M. Kirihara, N. Kuwamura, K. Taniguchi, and C. Hamaguchi

Department of Electronic Engineering, Osaka University,
2–1 Yamada-Oka, Suita City, Osaka 565
Telephone : (06)-879-7767

The feasibility of digital logic application of single electron tunneling devices is studied using a Monte Carlo circuit simulation. The simulational results revealed that (1) temperature should be below $e^2/40C_\Sigma k_B$ for stable digital logic operation, (2) "multi–electron" logics are more stable than ultimate "single–electron" logics in SET transistor circuits, and (3) propagation delay time as short as sub–n *sec.* can be achieved. With the aid of the Monte Carlo simulation, we proposed (1) a new NAND/NOR logic element with the use of two–input gate SET transistors and (2) a single electron memory cell composed of the NAND/NOR logic circuits. The logic operations were verified with the newly developed Monte Carlo simulation.

Introduction

The recent development of single electronic devices has exploited single–electron–tunneling phenomenon in coupled tunnel junctions. Although a number of topics relating to the physics on single electron tunneling have been studied, there is few quantitative studies on digital circuit application of single–electron devices.

The main purposes of this paper are twofold. First, we investigate the performance of the circuits reported by Tucker [1] using a Monte Carlo simulation. Second, we propose new logic elements using SET(Single Electron Tunneling) transistors such as a NAND/NOR logic gate and a single–electron memory cell.

The method of circuit simulation

A conventional circuit simulation is based on Kirchhoff's fundamental laws which cannot be used to simulate single electronic circuit because of the stochastic nature of tunnel events. We developed a SET circuit simulator using a Monte Carlo method taking into account the following features inherent in SET circuits; (1) electronic charge configuration in a network affects the electron tunneling rate and (2) the potential of each node changes discretely after a tunnel event.

The simulation of the single electron circuit is performed as follows. First, the electrostatic energy differences ΔE for all the tunnel capacitors before and after a tunneling event are estimated. Second, the average tunneling rates Γ of all the tunnel capacitors are calculated based on the following formula [2, 3],

$$\Gamma = \frac{\Delta E}{e^2 R_T [1 - \exp(-\Delta E / k_B T)]}$$

where R_T is tunneling resistance, k_B is the Boltzmann constant, and T is operation temperature. Third, the tunnel interval t is calculated using

$$t = -\ln(r)/\Gamma$$

where r is a random number distributed uniformly between 0 and 1. Fourth, only the shortest of the electron tunneling intervals is allowed and other tunneling events are discarded. The simulation time is advanced in accordance with the shortest tunneling interval and then the number of the electrons at the node is updated. The above processes are repeated until a given simulation time.

According to the Thèvenin's theorem, any circuit to which a tunnel junction of interest is connected is reduced to an equivalent circuit composed of an equivalent capacitor C_{ext} and a voltage source. After a tunneling event, the net charge on the node between the tunnel junction and the equivalent capacitor changes from n to n+1. The energy change ΔE accompanying the tunneling is given by

$$\Delta E = \frac{e(-ne + C_{ext} - e/2)}{C + C_{ext}} = \frac{e}{C}(|Q| - Q_c)$$

where Q_c is the critical charge [4] given by

$$Q_c = \frac{e}{2} \cdot \frac{C}{C + C_{ext}}.$$

Basic operation of inverter

Figure 1 shows the calculated output characteristics of an inverter switch consisting of two SET transistors and a load capacitor. Each switch consists of a set of two tunnel junctions and two normal capacitors. We assumed all the tunnel resistances to be 5 MΩ for simplicity. The abrupt changes of the calculated output characteristics represent the discreteness of electronic charge on the load capacitance; fifteen electrons make it full logic swing at the load capacitance of 360 aF. It should be noted that at very low temperature ($T = 5.16 \times 10^{-1}$ K), output voltage is quite stable, while it becomes unstable at higher temperature ($T = 5.16$ K), corresponding to 1/10 of the charging energy, due to thermal electron energy.

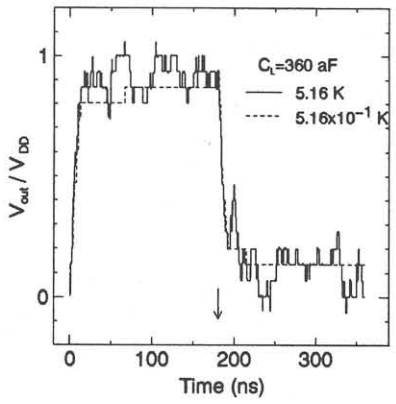

Figure 1: Calculated output characteristics of the inverter switch. Applied input voltage was switched from low– to high–level at the time indicating with an arrow.

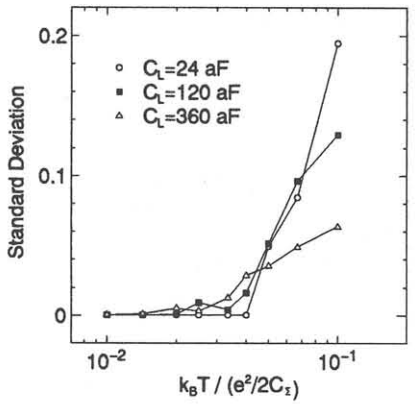

Figure 2: Standard deviation of output voltage fluctuation *versus* normalized temperature as a parameter of load capacitance.

Figure 2 shows standard deviation, σ, of the output voltage fluctuation *vs.* operation temperature as a parameter of a load capacitance, C_L. Note that for a circuit composed of 10^{10} inverter switches operating at 100 MHz, σ must be smaller than 0.05 to avoid erroneous logic operation for 10 years. This means that the operating temperature should be lower than $e^2/40C_\Sigma k_B$ regardless of the magnitude of the load capacitance, C_L. C_Σ is the sum of four capacitances composed of an SET transistor.

Figures 3(a)–(c) show calculated output characteristics of a three stage inverter chain. In Fig. 3(a), due to a small load capacitance C_L, both output voltage and oscillation period are quite unstable because node potentials and electron tunneling rates are strongly affected by the charge configuration of the next stage inverter. For more stable operation, larger load capacitance has to be used; this means that "multi–electron" logics ensures more stable operation than ultimate "single–electron" logics.

Basic logic circuits

The design methodology of CMOS circuits is not simply applicable to quasi–CMOS transistor logics [1]. For example, in NAND/NOR logic gates with three SET transistors connected in series, there occurs no tunneling in the center SET transistor because the electric potential of each node is greatly affected by each electronic tunnel event. Note that it is essential for electrons to tunnel through all the tunnel junctions for proper operations as NAND/NOR gates.

Figure 4 shows a newly proposed NAND/NOR logic gate consisting of two SET transistors with two input gate electrodes. For NOR logic operation, a driver SET transistor shown in Fig. 4 should turn off if both of the two input voltages are "low" while a load SET turn on. It is also possible that the function of the new device can be switched from NAND to NOR logic by simply exchanging the supply voltages, V_{DD} and the ground.

Random access memory cell

Figure 5 shows a new SET memory. The circuit enclosed with a dotted rectangle represents a SET–RAM cell which is similar to a three–transistor memory cell with separated input and output. There are four "wires" associated with each cell: write line (W.L.), write select (W.S.), read select (R.S.) and read line (R.L.).

Write cycle

With W.S. high, the lower SET transistor (T_2) is conductive for logic "0" and electrons are transferred to the memory capacitor, C_D, while for logic "1" electrons are transfered through the upper transistor (T_1), discharging the C_D.

Read cycle

For a read operation, the SET transistor (T_4) precharges the read line to logic "1" before the cell is accessed. After the R.S. is switched to "1", the read line remains high or is discharged depending on the data stored in the C_D. The rise/fall of the read line will then be detected by a sense amplifier.

The feature of this memory cell circuit is no need of refresh–process to retain data at a low temperature. Figure 6 shows data retention time as a function of operation temperature. The charge retention time is only several milli–second at 1.5 K, but below 0.5 K it would be practically infinite.

Conclusions

We proposed a new logic gates operating as a NAND/NOR gate and a storage cell for random access memory, whose functions were verified with a single–electronic circuit simulator using the Monte Carlo method.

In addition, the simulator predicted the followings: (1) propagation delay time as short as 10^{-10} sec. can be achieved in single–electronic circuit, (2) operation temperature should be less than $e^2/40C_\Sigma k_B$ to ensure stable logic operation, (3)"multi–electron" logics are preferable to "single–electron" logics for stable circuit operation.

References

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[2] H. Grabert, G.-L. Ingold, M. H. Devoret, D. Esève, H. Pothier, and C. Urbina, Z. Phys. B, **84**, 143 (1991).

[3] M. H. Devoret, and H. Grabert, in *Single Charge Tunneling*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992), p. 12.

[4] L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett., **64**, 2691 (1990).

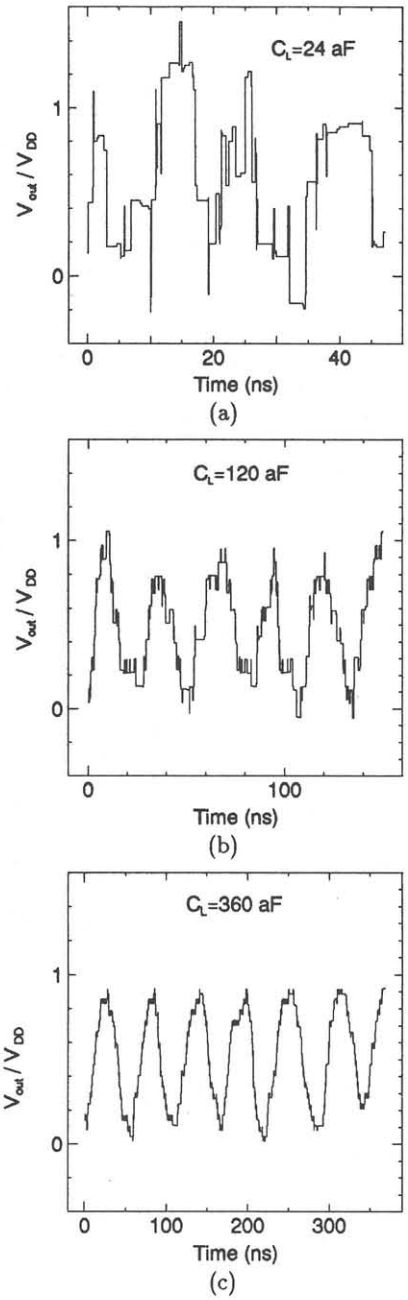

Figure 3: Calculated output characteristics of a three stage inverter chain for three different load capacitances.

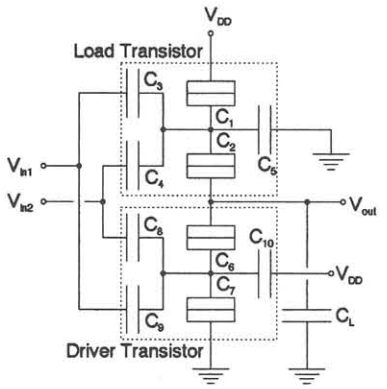

Figure 4: New NAND logic gate. The capacitances shown are C_1 =6.0 , C_2 =1.0 , C_3 = C_4 =2.5 , C_5 =10.0 , C_6 =2.0 , C_7 =1.0 , C_8 = C_9 =5.0 and C_{10} =4.0 aF. A tunnel junction is represented by a double box symbol.

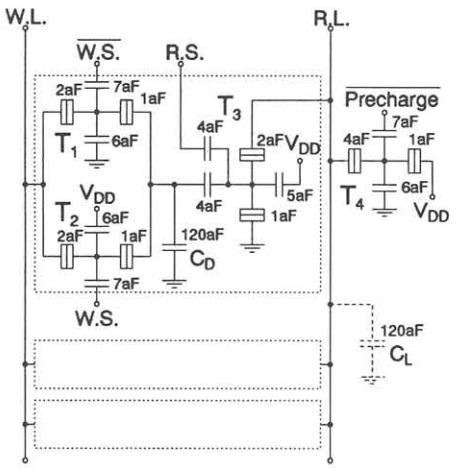

Figure 5: A SET memory cell circuit represented by the enclosed dotted rectangle.

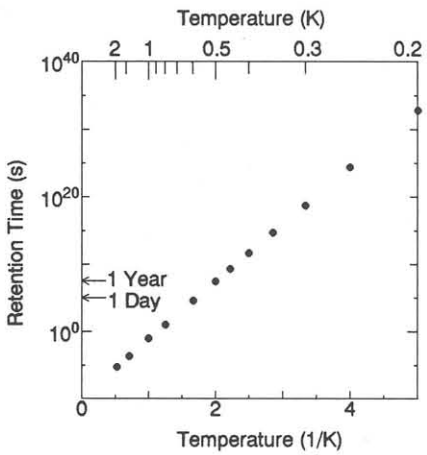

Figure 6: Data retention time *vs.* operation temperature.