Tunnel-Junction-Load SET Logic

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A novel tunnel-junction-load SET logic was proposed and its dynamics was analyzed. It was found that the proposed SET logic has the same simplicity as the resistance-load SET logic and the electron tunneling of the proposed SET logic is suppressed statically as in a complementary SET logic. The tunnel-junction-load SET logic is expected to become standard for future SET integrated circuits.

1. Introduction.

Many new devices using Single Electron Tunneling (SET) have been proposed recently and the dynamic characteristics are being investigated experimentally.[1-4]. Logic circuits using SET were proposed[1,2] because of its merit of high density and low power consumption. Conventional approaches were:

1) To utilize a load resistor for a pull-up circuit and a Capacitive Single Electron Transistor (CSET) for a pull-down circuit, namely, resistance-load SET logic as shown in Fig.1 (a) proposed by Likharev[1].

2) To utilize two CSETs for both pull-up and pull-down circuits, namely, the complementary SET logic as shown in Fig.1 (b) proposed by Tucker[2).

The output voltage in the resistance-load SET logic is unstable because the tunnel current flows statically when the output is low. On the other hand, the circuit of complementary SET logic is more complicated than the resistance-load SET logic just as a CMOS logic is more complicated than an nMOS logic.

In this report, we will propose a novel tunnel-junction-load SET logic to overcome these disadvantages and analyze its dynamics.

2. Tunnel-Junction-Load Logic

Figures 2(a) and (b) show the inverters of a proposed tunnel-junction-load SET logic. Each circuit consists of three tunnel junctions and gate/back-gate capacitances except for an output capacitance. Back-bias voltage $V_{bb}$ controls the input threshold voltage $V_{th}$. The proposed logic shown in Fig. 2(a) uses the tunnel-junction for a pull-up, while conventional SET logics need a CSET or a resistance for a pull-up. On the other hand, the circuit shown in Fig.2(b), which is another way of tunnel-junction-load SET logic, includes a tunnel junction as a pull-down and a CSET as a pull-up, respectively. In both circuits, a simple tunnel junction is used for pull-up or pull-down.

The tunnel-junction-load SET inverter in Fig.2(a) operates as shown in Fig.3. The internal state of the circuit is expressed by the excess charges $(q_A, q_B)$ at nodes A and B, respectively. When the input voltage $V_{in}$ is in the range between 0 and $V_{th}$, the internal state is $(0, 0)$ and the output is high. As the input voltage increases, the electron firstly tunnels at the junction $C_j$ and the internal state changes to $(0, -e)$. This state is also stable and the output is low when $V_{in}$ is in the range between $V_{th}$ and $V_{dd}$. The circuit in Fig.2(b) also operates like
increasing the input voltage

Coulomb blockade when \( V_{in} < V_{th} \)

electron \( \sim e \)

node B

Ground

state (0,0)

node A

Coulomb blockade when \( V_{in} > V_{th} \)

node A

state (0, -e)

node B

decreasing the input voltage

Fig 3. Operating principle of the tunnel-junction-load inverter.

where \( m_{ii} \) is the diagonal element of the matrix \( M \) and \( \mathbf{i} \) denotes the \( i \)-th element of a vector.

4. Calculation Results and Discussions

Figures 4(a) and (b) show the input-output characteristics obtained by the Monte Carlo simulation, which correspond to two types of circuits shown in Fig. 2(a) and (b). They are simulated under the condition of the temperature \( T = 0 \)K, 4mK and 8mK, respectively, where \( V_{dd} = 64 \)μV and \( C = 0.1fF \). Although both circuits can operate properly as shown in Figs. 4(a) and (b), the voltage gain decreases as the temperature rises in both circuits, which have the same characteristics because of their symmetric structure. \( V_{th} \) for Fig. 4(a) is given as

\[
F = \frac{1}{2} \mathbf{Q}_i^T \mathbf{M} \mathbf{Q}_i - \mathbf{V}_i^T \mathbf{Q}_i, \text{ and} \quad \mathbf{Q}_i = \left( \mathbf{Q}_{i1}, \mathbf{Q}_{i2}, \mathbf{Q}_{i3} \right),
\]

where \( \mathbf{Q}_i \) is the charge of electrons tunneling through the junction \( i \), \( \mathbf{V}_i \) is the constant vector determined by the source voltage and the prefix \( t \) denotes transpose of a matrix or a vector. The first term in Eq. (1) corresponds to the total amount of the electrostatic energy of all capacitances in the logic, and the second term corresponds to the work done by the voltage source. The electron tunneling is suppressed when the free energy of the SET logic increases compared with that before tunneling. Therefore, the condition of Coulomb blockade of the \( i \)-th tunnel-junction is given as

\[
\left| [\mathbf{M} \mathbf{Q}_i - \mathbf{V}_i]_i \right| > \frac{e}{2} m_{ii}, \quad (2)
\]

where \( m_{ii} \) is the diagonal element of the matrix \( M \) and \( \mathbf{i} \) denotes the \( i \)-th element of a vector. The condition of Coulomb blockade of the \( i \)-th tunnel-junction is given as

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\]

which can be derived from Eqs. (1) and (2). By substituting the circuit parameters to Eq. (3), \( V_{th} \) is calculated as 4.5μV, which agrees with the results in Fig. 4(a).

Figures 5(a) and (b) show the transient waveforms of input and output voltages of the circuit in Fig. 2(a). Here, simulation conditions are same as that in Fig. 4(a). It is noted that the electron tunneling is suppressed statically like a complementary CSET logic. Actually electrons tunnel across the tunnel-junctions at a finite tempera-
Fig. 4. Input-output characteristics of the tunnel-junction-load SET inverter. $C_1 = C_2 = C_3 = C_{in}/10 = C_B/10 = 0.1$ fF, $R_1 = R_2 = R = 100$ kΩ, $V_{dd} = 64$ μV, $T=8$ mK.

(b) Characteristic of the circuit shown in Fig. 2(b), $V_B=210$ μV.

5. Conclusion

We have proposed a novel tunnel-junction-load SET logic and analyzed its dynamics using Monte Carlo method. The proposed SET logic has the same simplicity as the resistance-load SET logic, and has the same stability as complementary SET logic because the electron tunneling of the proposed SET logic is also suppressed statically. The tunnel-junction-load SET logic is expected to become standard for SET integrated circuits in future.

References