Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 7-9

A-0-3

Invited

300mm Implementation

Frank Robertson
SEMATECH
2706 Montopolis Drive
Austin, TX 78741-6499

An internationally coordinated effort will be required to develop the capability to implement a larger wafer size and produce a viable market for 300 mm tools. Technology issues are largely understood and no insurmountable technical barriers are anticipated. A number of key challenges have been identified, and the industry must qualify potential solutions to achieve a 300 mm capability.

300 mm IMPLEMENTATION ENVIRONMENT

The semiconductor industry has prospered as a result of continuous productivity improvement over a long history. We have every reason to believe that this trend will continue into the foreseeable future. Periodic wafer size conversions, often funded by a lead company, have been an important element of the productivity improvement. However, the complexity and cost of implementing 300 mm are viewed as being beyond the resources of any one company. Our industry must cooperate in an international, precompetitive effort to succeed on such a scale.

Business issues have been the overriding concerns in 300 mm conversion, with the main question being the schedule for a critical mass of fab starts. Perception of a small total available market, the lack of opportunity for 200 mm / 300 mm transition equipment for most technologies, and uncertainty in the development funding model have greatly concerned the supplier community. The high cost of development has most companies analyzing their projections of return on that investment very carefully. A clear signal from the device manufacturers is needed that providing 300 mm capability will be a good business decision.

Despite the uncertainty, exploratory 300 mm work has begun in most quarters, with some suppliers moving aggressively to intercept a first wave of implementations in 1997 and 1998. The technology issues, while largely understood, require significant feasibility work to ensure that solutions are available. Though most processes will scale, some will need extensive modelling, control improvements or new architectures, and all must achieve extremely low defect densities. The high cost of large wafers adds a new dimension to the development and testing of equipment, which must be ready for cost-effective manufacturing when delivered.

The most aggressive implementation schedules drive the overall plan in Table 1.

First Silicon out	1Q98
Production Equipment Qualification	3Q97
Start Equipment Qual.	4Q96
Alpha Equipment Available	4Q95

Table 1. Schedule for 300 mm Implementation

The requirement of customers for production-worthy tools at delivery drives the use of IRONMAN $_{TM}$ and marathon demonstration methods which extend the traditional development cycle from 18-24 months to about 30 months. Project management analysis quickly verifies that those companies that wish to engage the early market should be well into their development efforts.

Equipment for 300 mm will initially target the 0.25 micron device generation, though early adopters will generally bring their fabs up on more mature (0.35-0.5 micron) products. The capabilities of equipment for this wafer size will be expected to improve to the requirements for 0.18 micron for early (circa 2001), though not the first, fabricators of that generation. It is anticipated that due to high development and implementation cost, 300 mm wafer size will have a longer life cycle than 200 mm.

General Requirements:
Defect density for immediate high yield
Minimal edge exclusion
Reliability hardware and software
Design for ergonomics
Conformance to international standards

Table 2a. General 300 mm Requirements

Equipment & Material-specific challenges:
Chem-Mechanical polish and uniformity cost
Etch uniformity
Thermal process control and wafer support
Silicon wafer quality and cost
Dielectric and metal deposition uniformity
Area-scanned process (litho, implant) throughput

Table 2b. Top Challenges for 300 mm Equipment and Materials

EQUIPMENT CONSIDERATIONS

Process control will be challenged by the size of 300 mm wafers at the same time as device electrical tolerances will drive very tight variability requirements. Defect densities and Overall Equipment Effectiveness (OEE) must support the need to maximize return on very high investment for 300 mm fabs. Electrostatic chucks will be key to minimizing edge exclusion losses. Standardization for carriers and interfaces will ease material handling approaches and cost of equipment, which must also be designed for ergonomics. These general equipment issues are among the top priorities for 300 mm development.

A number of technology-specific challenges exist which must be thoroughly analyzed to produce capable equipment. Thermal process temperature control and substrate support will be critical. Throughput of batch tools driven by wafer pitch, to accommodate larger diameter and maintain low thermal budget

through high ramp rates, will impact the cost of hot processes. Uniformity and cost of Chem-Mechanical Polishing (CMP) will become more important as more levels of metallization and application to shallow trench isolation are added.

Plasma source uniformity over large areas, charge build up and heat dissipation will be issues for both deposition and etch processes. Choice of surface preparation techniques (wet or dry process, in situ, clustering, wafer drying) must be integrated into the various process modules. The throughput of area-scanned processes such as Lithography and Ion Implant will drive tool architectures to minimize cost.

MATERIALS CONSIDERATIONS

The cost and quality of silicon wafers will be a foundation for device manufacturing effectiveness in the timeframe of 300 mm implementation. The cost of wafers is a significant driver of manufacturing cost and the control of wafer parameters a key determinant of yield, and thus the learning curves for these aspects will be key to implementing the larger size. The size of charge which can be thermally controlled, the fracture stress limit for the seed, speed of crystal pulling, ingot slicing and surface finish technique will all drive the economy of wafers.

After initial wafer processes, the cost and control of epi and thermal donor annihilation processes must be demonstrated. The interaction of subsequent device fabrication processes with silicon wafer mechanical, chemical and electrical properties must be taken into account in the design of both equipment and process recipes. Particular attention must be paid to oxygen content, thermal ramp rates and wafer pitch to avoid plastic deformation and dislocations [1,2,3,4]. Surface preparation techniques and thermal cycles must be optimized to maintain surface microroughness consistent with high gate dielectric integrity.

CONCLUSION

The implementation of 300 mm capability to continue improvement in productivity will occur over the next several years, and will require collaborative effort on an unprecedented scale. Though technical issues can likely be addressed, there are a number of challenging problems for large wafers. Engineering must comprehend equipment performance, materials properties and device needs.

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