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Super-β Bipolar Transistor Equivalent in CMOS Technology

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A CMOS circuit equivalent to a super-β bipolar junction transistor is proposed. The equivalent provides symmetrical performances of NPN/PNP, programmable ideality factor which can compensates the degradation of junction quality from scaled technologies. The prototype fabricated in $0.8\mu m$ CMOS technology showed 2.3×10^{-16}A of I_S, $2.4mA$ of I_{KF}, $390V$ of Early voltage, and infinite β at DC. Advantages and disadvantages compared to typical bipolar transistors are discussed.

1. INTRODUCTION

Each MOS transistor in CMOS technology has p-n junctions. The attempts to get a bipolar junction transistor(BJT) in CMOS technology have been focused on making a real NPN or PNP structure with these junctions [1]. If an MOS transistor network can emulate the collector action, an equivalent of BJT can be obtained with a p-n junction.

In this paper, a super-β bipolar transistor equivalent in CMOS technology is proposed. The equivalent provides designable ideality factor, β, and output impedance respectively in CMOS technology. The proposed circuit compensates the junction quality degradation from scaled technologies. A prototype implementation of the concept was fabricated with a standard $0.8\mu m$ CMOS technology without any process modification and showed the predicted characteristics.

2. CONCEPT OF THE EQUIVALENT

The concept of the super-β bipolar transistor is shown in **Fig.** 1. The feedback loop composed of the amplifier and the MOS transistor sets the node potential of the internal base B' with that of B. Hence the B-E voltage is applied to the diode. The current into node C is an exponential function of V_{BE} and independent of the potential of node C, which gives large output impedance. Hence the nodes C, B, and E correspond to the collector, base, and emitter respectively.

This concept can be implemented into the circuits in **Fig.** 2 (a) and (b) for NPN and PNP respectively. A voltage mirror is formed with the transistors M_1-M_4. The cascode transistor M_5 corresponds to the MOS transistor of **Fig.** 1. M_2 and M_5 comprise the gain-boosted cascode for high output impedance [2].

The diode D is formed using the source/drain diffusion in a well. Without proper annealing, some of the shallow junction formation technology which is common for scaled MOS technologies such as preamorphisation [3] degrades the quality of junction. The ideality factor programmability of this equivalent overcomes the junction quality degradation.

Ideality factor is a parameter of a fabrication technology. When the junction is ideal, the ideality factor is unity(it cannot be smaller than one in any case, as this would indicate that the junction is better than perfect) [4]. In this equivalent concept, the ideality factor can be designed to even below unity by the size ratio of the transistors M_1 and M_2, and M_3 and M_4. The Gummel plots in **Fig.** 3 show some examples of ideality factor design. With this feature, even with degraded quality junction diode, a proper bipolar transistor can be built.

The size control of the effective emitter is another problem. A design technique is developed to control the emitter size without process variation. **Fig.** 4 is a

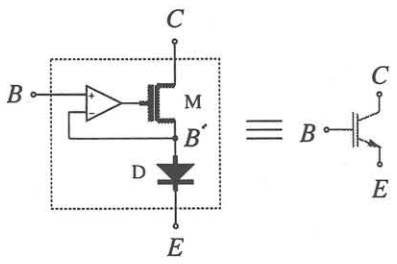

Fig. 1. **The Equivalent Concept.**

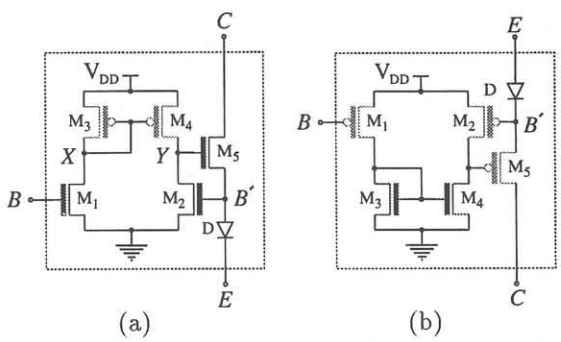

Fig. 2. **Circuit Implementations of The Equivalent Concept.** (a) NPN. (b) PNP.

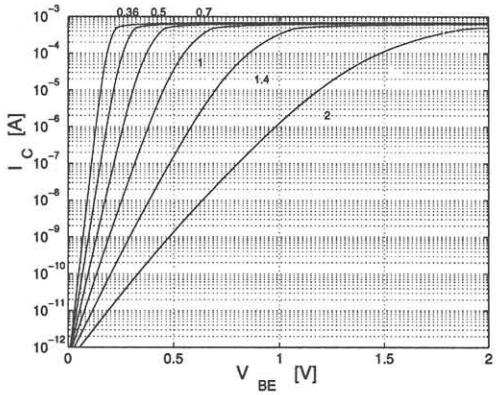

Fig. 3. **Gummel plot of the BJT equivalent with various ideality factors.** $I_{KF} = 680\mu A$. Examples show the ideality factor of 0.36, 0.5, 0.7, 1, 1.4, and 2.

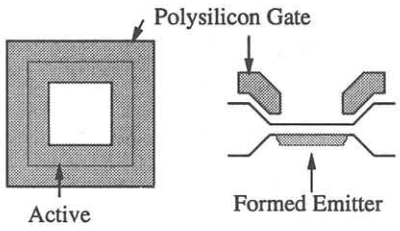

Fig. 4. **Technique for the Control of effective Emitter Size.**

simplified diagram of the technique. The gate polysilicon works as the ion implantation mask for the emitter. Symmetrical design reduces the deviations from misalignment and ion implantation.

The main component of the base current of this equivalent is the displacement current through the gate capacitance of M_1. This component makes a pole at DC in the β characteristics. It operates as a low pass filter for the input signal and can cause phase margin problem when this equivalent is used in feedback circuitry. **Fig.** 6 shows two ways to alleviate this problem. One is bleeding technique, as shown in **Fig.** 5. The bleeding resistor provides a DC current path for the base current, making the β curve flat. The other is making a feed-forward path between the equivalent base and the anode of the diode as in **Fig.** 6. Since the anode potential will track the potential of the base, smaller resistance can be used for the same bandwidth than bleeding. **Fig.** 7 shows the result of this flattening. The feed-forward resistor can be replaced with an MOS transistor which operates in linear region. This replacement offers another degree of freedom in circuit design — programmable β.

3. RESULTS AND DISCUSSIONS

The prototype of this concept was fabricated with a $0.8\mu m$ CMOS technology. **Fig.** 8 is the microphoto-

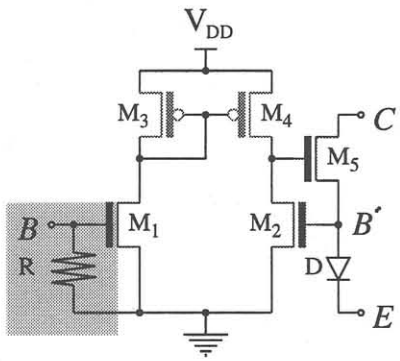

Fig. 5. β flattening technique I - Bleeding.

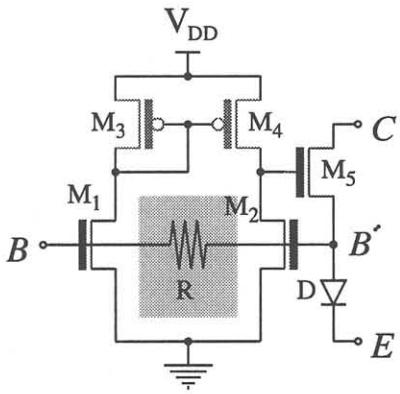

Fig. 6. β flattening technique II - feedforward.

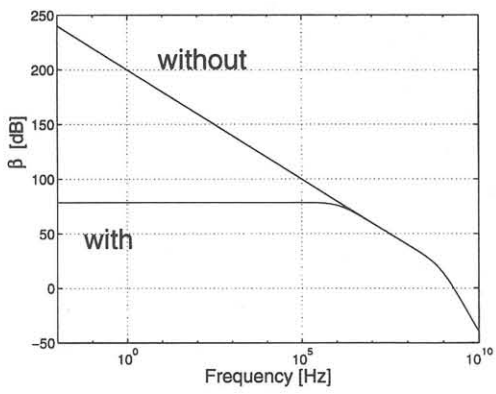

Fig. 7. β versus Frequency. Before and after the flattening. Simulation result with a $0.8\mu m$ CMOS technology.

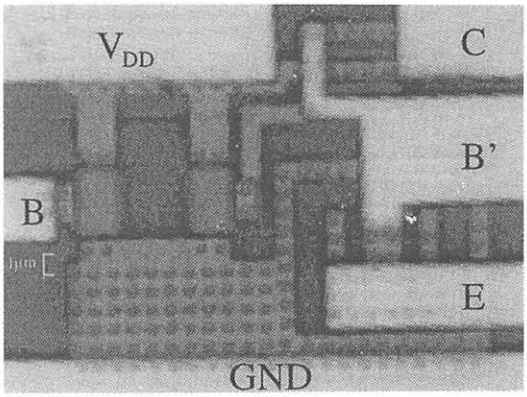

Fig. 8. **Microphotograph of the Prototype.**

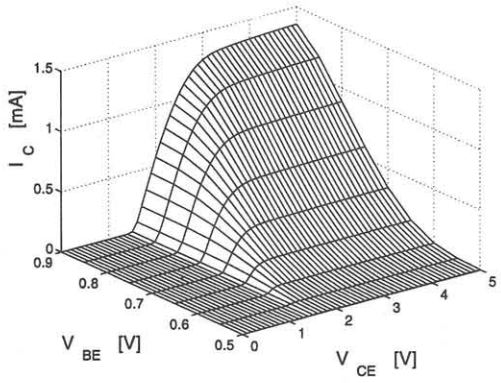

Fig. 10. **Measured $I-V$ characteristics of the fabricated Prototype.**

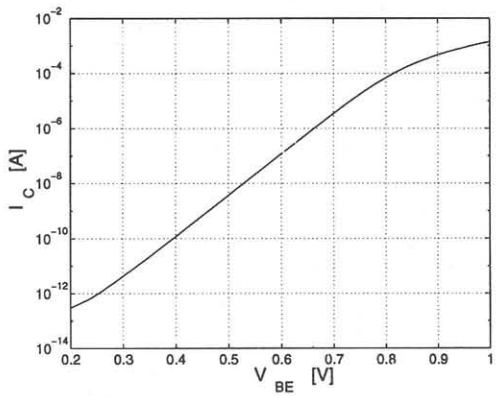

Fig. 9. **Measured Gummel plot of the fabricated Prototype.** Note the absence of the base current curve. $I_S = 2.3\times10^{-16}A$.

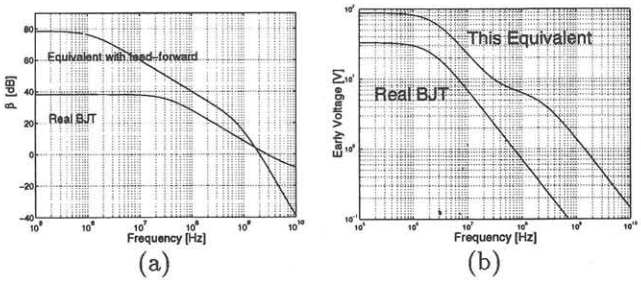

Fig. 11. **Comparison of the Characteristics in simulation.** (a) β. (b) Early Voltage.

graph of the prototype. **Fig.** 9 is the measured Gummel plot of the prototype which shows the bipolar action of this prototype. I_S is 2.3×10^{-16}A, and I_{KF} is $2.4mA$.

I-V characteristics of the prototype are in **Fig.** 10. Exponential nature on V_{BE}-I_C and high output impedance show the characteristics of BJT action. The shift on the V_{CE} axis results from the operation of M_5. The measured Early voltage is 390V.

Fig. 11(a) shows β's of this equivalent and a typical NPN transistor. The equivalent shows superior β up to around 1.65GHz in this figure. In a $0.8\mu m$ CMOS technology, a cut-off frequency of 0.5 to 2.7GHz can be obtained. **Fig.** 11(b) shows output impedances of this BJT equivalent and a typical NPN transistor.

Table I is the measured characteristics summary of the fabricated prototype.

Although this equivalent shows many advantages over the normal bipolar transistor, since this equivalent is made of MOSFET network, it has some disadvantages as well. This equivalent shows higher noise level than typical NPN transistors from the MOSFET network, The early saturation which is found in **Fig.** 10 puts a limit on low-voltage application of this equivalent.

4. CONCLUSION

A super-β bipolar transistor equivalent in CMOS technology is proposed. The ideality factor programmability makes it possible to compensate the degradation of junction quality in scaled technologies. With this Concept, high β, high output impedance, symmetrical NPN and PNP devices, and programmable ideality factor can be obtained with a standard CMOS technology.

References

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2) B.-S. Song, *CMOS Analog System Design*, p. 57, ISRC, Seoul National University, Seoul, Korea, 1991.
3) S. J. Kwon, H. J. Kim, and J. D. Lee, "Shallow p^+-n Junction Formation by As^+-Preamorphization and Field-Retarded Diffusion", *SSDM '90*, Sendai, Japan, pp. 413-416, 1990.
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TABLE I

Characteristics summary of the fabricated Prototype.

β	∞
V_A[V]	390
$I_{KF}[mA]$	2.4
$I_S[A]$	2.3×10^{-16}