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CVD-EPI MOS Transistors with a 65 nm Vertical Channel

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Optical lithography is expected not to be suitable for fabrication of planar structures in the sub 0.1 µm range. In a vertical technology the channel length can be defined by the thickness of CVD-EPI layers, which can be grown on nanometer scale. Because here is no limit by lithography even transistors with 65 nm channel length can be fabricated using conventional lithography. The electrical parameters of vertical devices are comparable to planar transistors. Especially for the shortest channel length high saturation currents are observed. Furthermore the vertical transistor technology has the ability for higher integration density.

1. Introduction

Vertical MOS transistors offer the attractive perspective to reduce the channel length and the device area without the need for sophisticated lithographic equipment. The channel length of a vertical MOS transistor is defined by the thickness of an epitaxial layer which can be very well controlled down to nm-dimension. In the vertical transistor technology it is relatively easy to fabricate transistors with channel length smaller than 0.1 µm. In principal the complete transistors, source, channel region and drain could be grown in a single CVD chamber thus reducing process complexity.

2. Device Fabrication

After fabricating an experimental version of a vertical NMOS transistor with epitaxial layers grown by MBE [1], the transistors described below were processed in a production line environment using CVD-epitaxy. The schematic cross section of a vertical MOSFET and a SEM picture of the channel region are shown in Figs. 1 and 2, respectively. By using a mesa-type device, the lengths of all four side-walls contribute to the total channel width resulting in an area reduction of about two compared with planar devices.

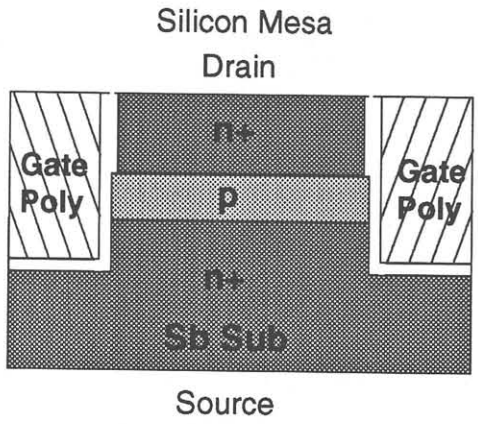

Fig. 1 Schematic cross section of a vertical NMOS transistor

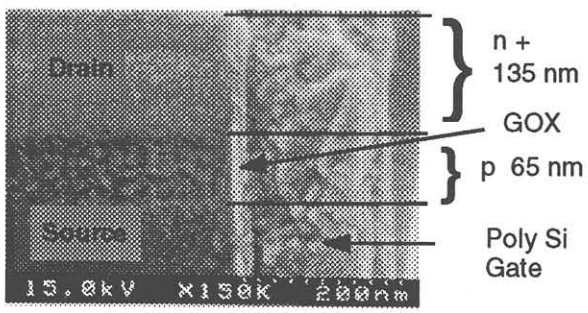

Fig. 2 SEM picture of channel region of vertical NMOS transistor (L = 65 nm)

As an example the process flow for vertical transistors with 400 nm channel length is given below. The process was started with field isolation followed by low pressure chemical vapor deposition (LPCVD) at 900° C with $Si_2H_2Cl_2$ and B_2H_6 on highly doped (20 mΩcm) Sb-wafers. The boron doping concentrations for threshold voltage adjust as well as for anti-punch-through was $2*10^{17}$ cm^{-3}. The drain region was formed by ion implantation of Arsenic (50 keV, $5*10^{15}$ cm^{-2}) resulting in a depth of approximately 200 nm at the end of the process. This implantation defines, together with the thickness of the epitaxial layer, the channel length of the device. The total thickness of the epitaxial layer was 600 nm resulting in a channel length of 400 nm. Subsequently, a shallow trench with 0.8 µm depth was etched through the epitaxial layer down to the n-substrate. Next process step was dry thermal oxidation of the gate dielectric at 825° C with a thickness of 12 nm. A relatively low temperature of 825° C was chosen for the

gate oxidation to minimize outdiffusion of the Boron doping. Then, a 200 nm thick poly-Si layer was used for the gate and doped with Phosphorus. Finally, BPSG dielectric was deposited, followed by contact hole etching, Tungsten fill and Aluminum wiring. The annealing and activation after ion implantation and the reflow of the interlayer dielectric were done simultaneously by thermal annealing at 900° C for 60 min. The total mask count was only five. The process flow is summarized in Table 1.

Table 1

Substrate: Sb doped, 20 mΩcm
1. Photolithography (LOCOS process)
   CVD epitaxy (Boron doped)
   n+ -implantation (As, 50 KeV, 5.10^{15} cm^{-2})
   TEOS deposition
2. Photolithography (patterning of TEOS)
   RIE etching of trench
   Gate oxidation
   Poly-silicon deposition and implantation (Phosphorus)
3. Photolithography (patterning of poly-silicon)
   RIE etching of poly-silicon gate
   Deposition of interlayer dielectric
   Thermal anneal
4. Photolithography (contact holes)
   RIE etching of contact holes
   Sputtering of barrier and deposition of tungsten
   Sputtering of AlSiCu metalization
5. Photolithography (patterning of metal)
   Forming gas anneal 450°C

3. Long Channel Device Characteristics

The drain current characteristics for 400 nm channel length is given in Fig. 3. A transconductance of 135 µS/µm is reached that compares well with planar devices of similar geometry. The threshold voltage is 0.5V and the subthreshold slope is 80 mV/dec and a drain induced barrier lowering (DIBL) of 30 mV/V_{DS} was measured. For voltages V_{DS} > 3.0 V, an increase of the drain current is observed caused by charging of the floating bulk region of the MOS transistor due to the substrate current. This mechanism resembles the 'Kink'-effect of SOI-transistors. The subthreshold current shows good turn-off behavior (Fig. 3). But the carrier generation in the floating bulk region increases the current for greater V_{DS}. Generally, the floating bulk is of minor impact on the functionality of vertical MOS devices at low operation voltages typically for short channel transistors. The performance could be increased if a buried n+ layer is implemented to the process [2].

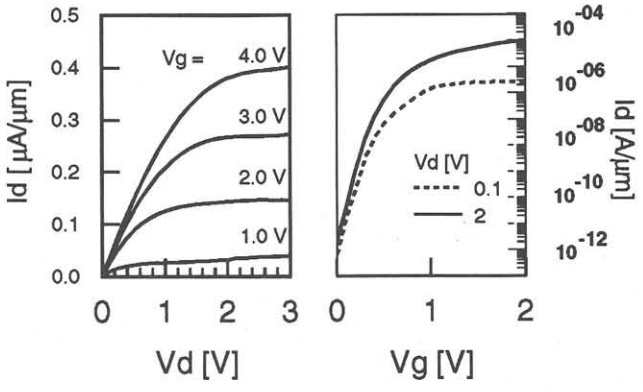

Fig. 3 I(V)-curves of vertical NMOS transistor (L = 400 nm) in the active and subthreshold region

4. Doping Profiles and Device Characteristics of Short Channel Vertical Transistors

To show the potential of vertical MOS technology, NMOS transistors with a channel lengths below 100 nm have been fabricated. In a similar way as for the long channel transistor the short channel vertical transistors were processed. Here a lower thermal budget has to be used resulting in a depth of the As doping of approximately 135 nm at the end of the process. The Boron doping of the channel EPI-layer was increased to $2*10^{18}$ cm^{-3} and the thickness was varied from 200 to 300 nm resulting in channel lengths from 65 to 170 nm. After a trench etching of 0.3 to 0.5 µm gate oxidation of 5 nm followed. For annealing and activation a rapid thermal anneal at 900 °C for 60 sec was used. SIMS doping concentrations of As and B for the 65 nm vertical transistor are shown in Fig. 4.

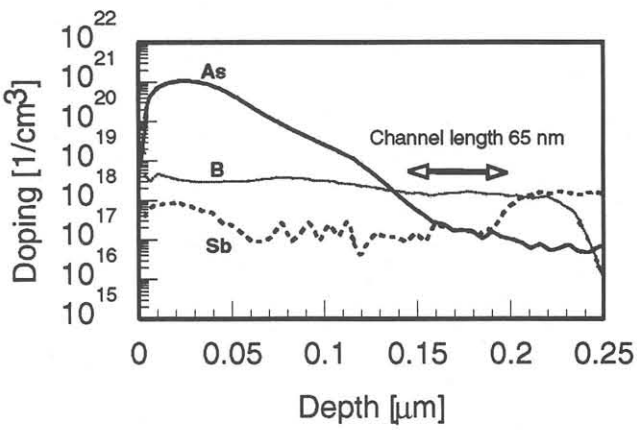

Fig. 4 SIMS-profile of the drain, channel and source region for a 65 nm vertical transistor

In Fig. 5 the subthreshold current of three short channel devices is given. The threshold voltage at low drain voltage (V_{DS} = 0.1V) is 0.8V (L=170 nm), 0.6V (L= 120 nm) and 0.4V (L=65 nm). The threshold voltage was not adjusted to the channel length as all three devices had the same doping concentration in the EPI-layer. The subthreshold slope degrades for our vertical transistors with decreasing channel length and is slightly worse than in planar transistors. This higher slope is due to damage during the trench etching process without further additional annealing steps. The DIBL voltage is also increasing with decreasing channel length and gives 250 mV/V_{DS} for the shortest device. This effect is known from short channel SOI devices [3].

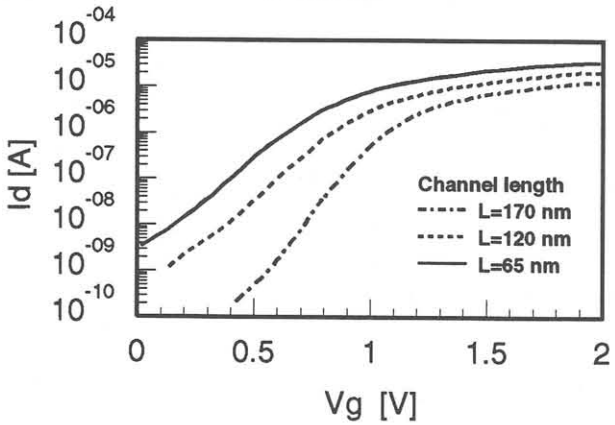

Fig. 5 Transfer characteristic at low V_{DS} with decreasing channel length

In Fig. 6 I-V curves of three transistors with extremely short channel length (L=170 nm, L=120 nm and L= 65 nm) are shown for V_G=2V. The high saturation currents demonstrate the potential of the vertical technology. Even devices down to 65 nm channel length are working very well. The increase in current for the shortest device with respect to the 120 nm transistor is attributed to the strong barrier lowering at source and to the 'Kink' effect for higher drain voltages. The I-V characteristics are given in more detail in Fig. 7.
A saturation current of 350 µA/µm is obtained at low operation voltages V_G = V_{DS} = 1.5 V. The kink effect caused by the floating body of this device is clearly to be seen. This effect is starting at V_{DS} = 1.5 V due to avalanche generation of holes. This additional current contributes to the increasing saturation current at higher drain voltages.

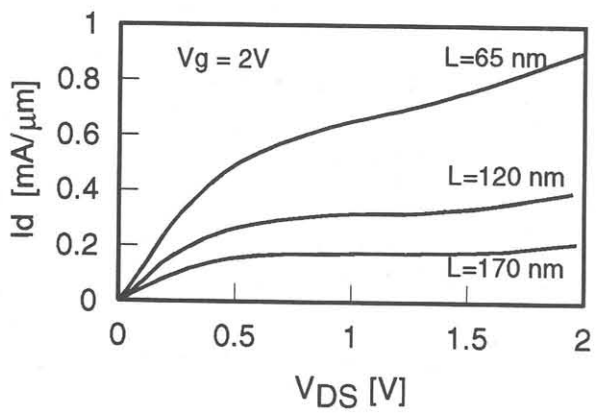

Fig. 6 Drain current at V_{GS} = 2 V with decreasing channel length

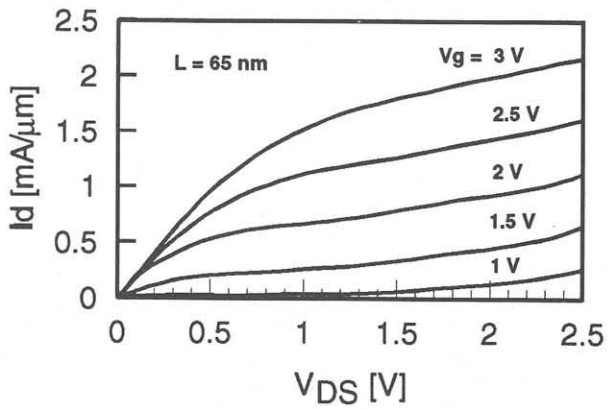

Fig. 7 I_D-V_{DS} characteristics of vertical NMOS transistor (L = 65 nm)

5. Conclusion

Vertical NMOS transistors with channel lengths down to 65 nm have been fabricated using LPCVD-epitaxy. The vertical transistors show good electrical characteristics. Thus, transistors with high current drive due to very short channel lengths and reduced area due to the 3D stack become manufacturable using still i-line lithography technique. First results are very promising and demonstrate the potential of the vertical transistor technology for channel lengths of 100 nm and below.

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