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Polysilicon Thin Film Transistors with PN Junction Gate

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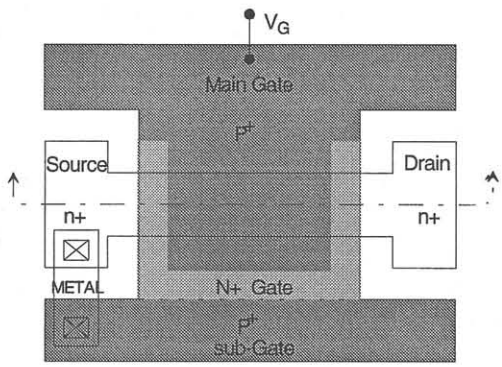
We propose and fabricate a new polysilicon thin film transistors (poly-Si TFTs) which exhibit the properties of an offset gated structure in OFF state, while acting as a non-offset structure in ON state. The fabrication process is compatible with the conventional non-offset poly-Si TFT process and does not require any additional mask. Our experimental results show that the leakage current of the new device is two orders of magnitude lower than that of the non-offset device, while the ON current of the new device is almost identical with that of the non-offset device. It is found that the ON/OFF current ratio is improved remarkably.

1. INTRODUCTION

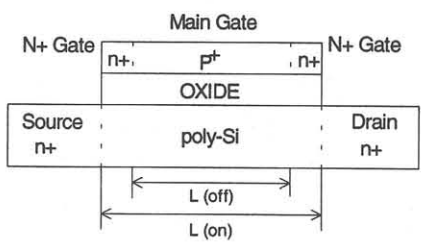
One of the problems of polysilicon TFTs, which exhibits the large mobility and ON current, is a large OFF state leakage current. [1] Various LDD structures and offset gated structures have been proposed to suppress the leakage current by reducing the drain field. [2) 3)] However, the ON current for these structures is usually decreased due to the extra series resistance caused by the offset region. [4)] It is desirable to have a device which would exhibit an offset gated structure in the OFF state and behave like a non-offset device in the ON state. [5)] The purpose of our work is to report a new thin film transistor with pn junction gate in order to suppress the leakage current during the OFF state without sacrificing the ON current during the ON state.

2. DEVICE STRUCTURE

The key feature of the new structure, as shown in Fig. 1, is that the gate is composed with pnp junction. The N^+ doped part of the gate, which we define as the N^+ gate, overlays the channel region near the drain and source. The main gate and subgate part of the gate are composed of the P^+ doped region. The gate voltage is applied to the main gate and the subgate is connected to the source. In the OFF state ($V_S > V_G$), the source voltage is applied to the N^+ gate through the forward biased pn junction. The source voltage is isolated from the main gate because the reverse biased pn junction is formed inherently between the N^+ gate and the P^+ doped main gate. As the gate voltage decreases, the N^+ gate region is equal to V_S (which is a constant voltage) and prevents the increase of the vertical electric field between the drain and the gate. Then, as the gate voltage decreases, the leakage current does not increase and remains constant. In the ON state ($V_S < V_G$), the gate voltage is applied to the N^+ gate through forward biased pn junction and the gate voltage is isolated from the subgate. Therefore, the N^+ gate voltage is equivalent to the main gate voltage, so that the new device acts as the non-offset device in the ON state.



(a) Top View



(b) Cross-section

Fig. 1 The schematic feature of the new TFT
(a) Top view (b) Cross section

In order to verify the proposed poly-Si TFTs, we have simulated the potential distribution in the gate under the ON state and the OFF state, as shown in Fig. 2. The

simulation results indicate that the gate voltage is applied completely to the N^+ gate in the ON state and only to the main gate alone in the OFF state. This indicates that the N^+ gate region acts as the offset region under the OFF state, which results in the reduction of the gate length.

It is observed in Fig. 3 that the maximum OFF state electric field in the new device is approximately half of the non-offset device, which indicates that the leakage current of the new device should be smaller than that of the non-offset device.

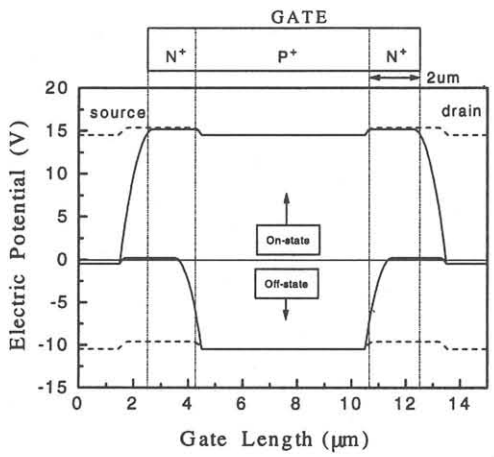


Fig. 2 The potential profile within the gate of ON state (V_G=15V, V_S=0V) and OFF state (V_G=-10V, V_S=0V) in the new device with N^+ Gate=2um. The dotted line represents the potential profile when the subgate and the source are disconnected.

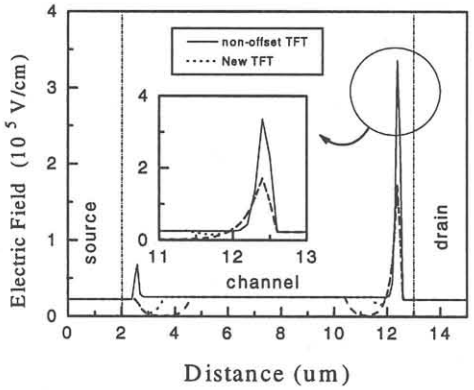


Fig. 3 The OFF state electric field along the channel at V_G=-10V and V_D=5V.

Fig. 4 shows the electron concentration along the channel in the ON state of the new device is two orders of magnitude higher than that of the conventional offset device and the same as of the non-offset device, which implies the ON current of the new device should be almost identical with that of the non-offset device.

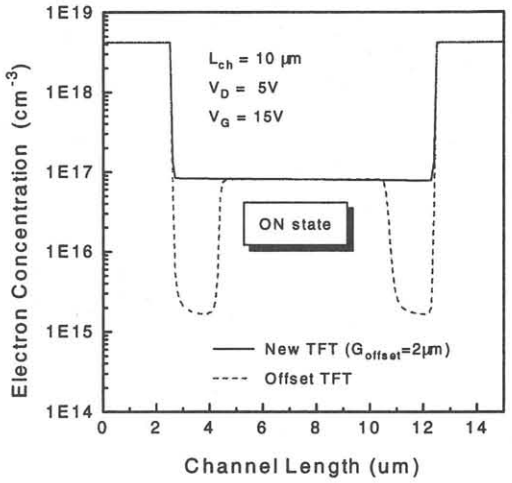


Fig. 4 The electron concentration along the channel in OFF state for the conventional offset device and the new device.

3. EXPERIMENTS AND RESULTS

We have fabricated the proposed poly-Si TFTs with the N^+ gate length of 2μm and the non-offset TFTs, using a low temperature process. The process sequences of the new device are same as of the non-offset device, except that the N^+ and P^+ implantation photolithographic steps.

The main process sequences of the new poly-Si TFTs are as follows. Silicon wafers with 5000Å thermally grown oxide are used as starting substrate. Undoped 1000Å thick amorphous silicon (a-Si) films are deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. The a-Si film is then crystallized during a 30-hour anneal at 600°C. After forming silicon islands, the gate oxide and the gate polysilicon with the same thickness of 1000Å are deposited and patterned. The process sequences prior to the gate pattern for the new device are same as for the conventional non-offset device. For N^+ and P^+ implantation photolithographic steps, as shown in Fig. 5, N^+ ion impurities are implanted into the n-type forming region (for nMOS, the source/drain region and the n^+ gate part of the gate and for pMOS TFT, the n-type main gate and subgate). P^+ ion impurities are then implanted into the p-type forming

region, which is the masked region in the N^+ ion implantation step. The isolation oxide is deposited, followed by the dopant activation anneal at 600 °C for 20 hours. Finally, a contact etch and an aluminum formation are carried out.

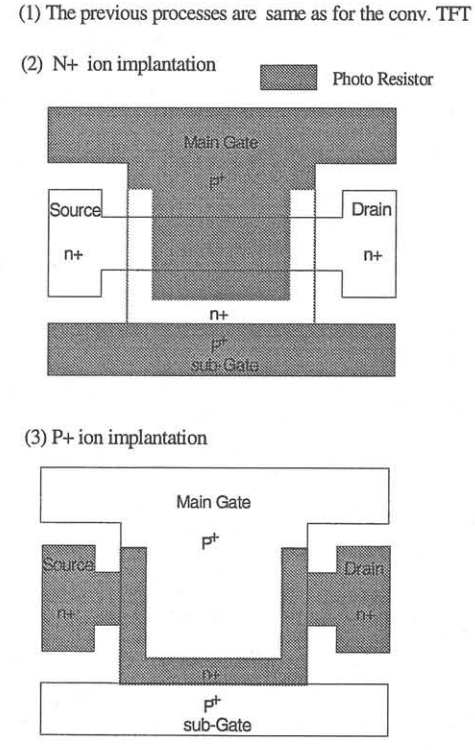


Fig. 5 The implantation steps of n-type TFT. For p-type TFT, the implantation region and the PR masked region for n-type TFT are reversed each other.

It is observed, as shown in Fig. 6, that ON current of the new device is almost same as that of the non-offset device. As the gate voltage decreases, the increase of the leakage current of the new nMOS is smaller than that of the non-offset nMOS. The leakage current of the new device is two orders of magnitude lower than that of the non-offset device at V_G= –20V. For the new pMOS, it is observed that the leakage current does not increase at all with the gate voltage. In the pMOS, the small drain voltage (V_D=5V) does not have an effect on the increase of the leakage current due to the low hole mobility. It is also found that the ON/OFF current ratio is increased significantly by two orders in the new device.

4. CONCLUSIONS

We have fabricated a new poly-Si thin film transistor of which the leakage current is reduced in the OFF state without sacrificing the ON current. The new device does not require an additional process step, which is identical with the fabrication of the conventional device. We have also observed that the ON/OFF current ratio is increased significantly by two orders in the new device.

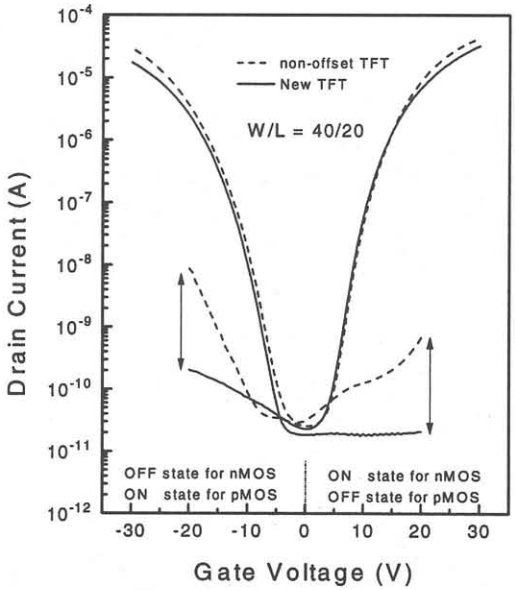


Fig. 6 The measured I_D-V_G curves of the new TFT and the non-offset TFT at V_D=5V, N^+ gate=2um

ACKNOWLEDGMENT

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