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# In-Situ Doped CMOS Polysilicon Thin Film Transistors

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We have fabricated the novel poly-Si TFTs employing in-situ doping process to implement poly-Si CMOS TFT technology, which do not require an additional impurity activation. With the new devices, we have observed excellent electrical characteristics of ON/OFF current ratio of about $10^7$ and the remarkable reduction of kink effect due to the very thin channel layer. Also, the new device structure may reduce one photo-lithographic step less than the conventional one and the fabrication process is simple.

## 1. INTRODUCTION

A conventional ion implantation technique may not be suitable for large area Active Matrix Liquid Crystalline Display (AMLCD) because the uniformity decreases significantly as the substrate size increases. [1) 2)] Furthermore, the implantation requires an additional impurity activation annealing to form the source and drain region of TFTs. Especially, in low temperature poly-Si TFTs, the long annealing time leads to lower production yield.

In this paper, we have proposed and fabricated the new poly-Si TFTs with in-situ doping process to form n- and p-channel device which does not require any impurity activation on the same substrate. Compared with the conventional device, the new device structure may reduce one photo-lithographic step and fabricate the very thin film transistors which reduce kink effect considerably.

## 2. EXPERIMENTS AND RESULTS

The main processing sequences of the new device is illustrated in Fig. 1. Doped n+ amorphous silicon (a-Si), lower buffer oxide, doped p+ a-Si and upper buffer oxide with the same thickness of 100nm are deposited sequentially by LPCVD on thermally oxidized silicon substrates at 550°C.(a) [3)] The upper oxide layer and p+ doped a-Si are formed with an p+ active mask.(b) Subsequently, the lower oxide layer and the n+ doped a-Si are formed with n+ active mask.(c) It is noted that the channel region of the devices is etched simultaneously at this time. Another undoped 30nm thick a-Si film is deposited and crystallization is performed at 600°C for 30 hours in $N_2$ ambient. Gate oxide and poly-Si gate of 100nm are deposited by LPCVD.(d) The above four layers, such as poly-Si gate, gate oxide, 30nm poly-Si and buffer oxide, are etched by using a gate mask which is overlapped with the n+ and p+ doped poly-Si layer.(e) The isolation oxide is deposited. Finally, a contact etch and an aluminum formation are carried out.

The measured $I_D$-$V_G$ curves of the new n-channel devices show the leakage current of below 10 pA and the maximum ON/OFF current ratio is about $10^7$, as shown in Fig. 2. The $I_D$-$V_G$ curves for the p-channel devices show the same trend in a lesser degree. The $I_D$-$V_D$ curves of Fig. 3, indicate that the kink effect is suppressed considerably under the large gate voltage due to the very thin channel layer. The reduction of kink effect may be explained that the new device acts as a fully-depleted SOI device because the channel thickness (30nm) of the new device is thinner than that (100nm) of the conventional device. It is well known that the kink effect may be diminished as the channel thickness decreases. It is another merit that the over-etch problems of contact hole may be overcome because the source/drain region (the doped poly-Si) can be made thick maintaining the very thin channel layer (the channel poly-Si) and the very thin film transistors may be fabricated easily.

In this work, hydrogenation passivation is performed in a plasma reactor for various periods. [4)] The hydrogen plasma treatment conditions are 300°C and 0.5 Torr. The power density is 0.25 W/cm$^2$ at the frequency of 13.56 MHz. The hydrogenation effects on the new poly-Si TFTs are compared with that of the conventional poly-Si TFTs. It is observed that the hydrogenation effects depend on the active poly-Si layer thickness difference between the new device and the conventional device, as shown in Fig. 4. [5)] Compared with the conventional device, the device characteristics, such as threshold voltage, field effect mobility and subthreshold swing, are significantly improved with hydrogenation period. It is found that the active layer thickness of the device plays the key role for the hydrogenation passivation.

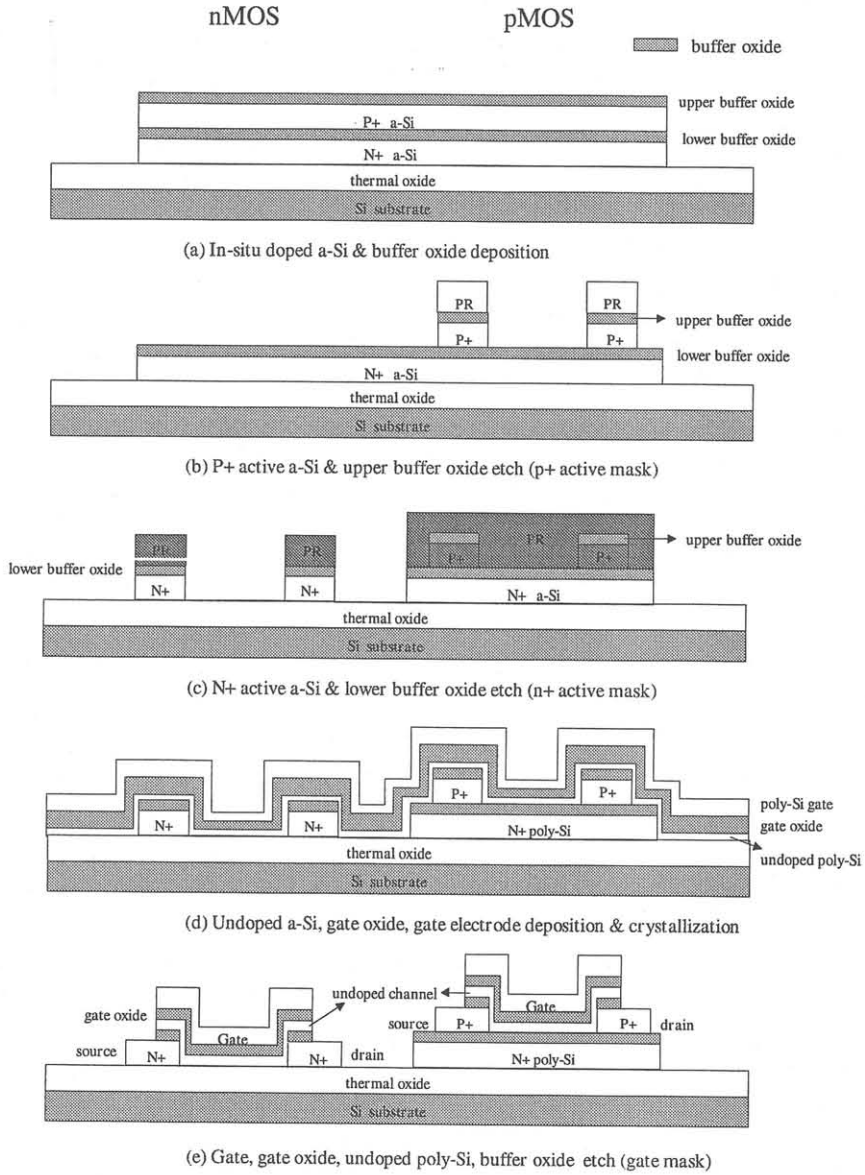


Fig. 1 Main processing steps for the new CMOS TFTs

## 3. CONCLUSIONS

We have successfully fabricated the novel poly-Si TFTs by employing in-situ doping process to implement poly-Si CMOS TFT technology. The proposed process is suitable for the large area display and also does not require any additional impurity activation. With the new devices, we have observed excellent electrical characteristics of ON/OFF ratio of about $10^7$ and the remarkable reduction of kink current due to the very thin channel layer. The another merit of the device is that the device structure can reduce one photo-lithographic step less than the conventional one. Compared with the implantation process, the in-situ doping method is expected to be able to produce the large area display because the large area doping is obtained easily.

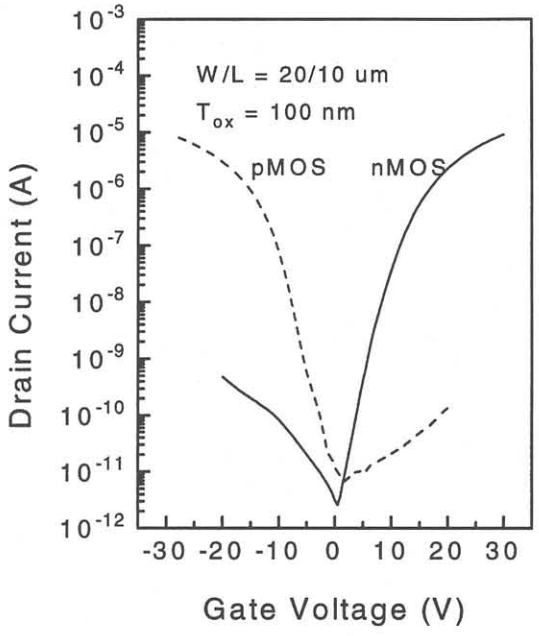


Fig. 2 $I_D$-$V_G$ curves for the new poly-Si TFTs (nMOS and pMOS).W/L=20/10 um, $V_D$=5V.

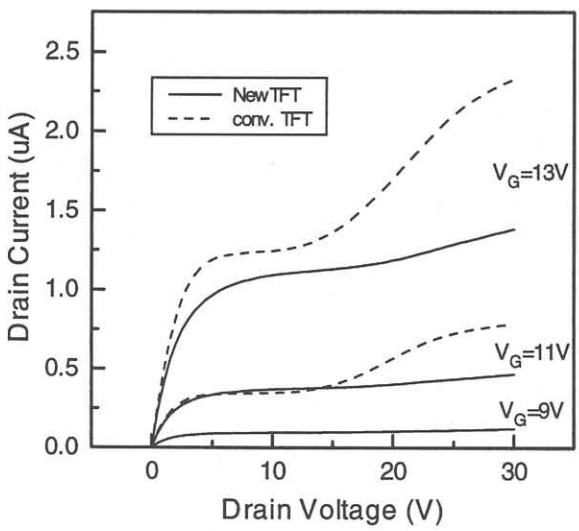


Fig. 3 $I_D$-$V_D$ curves for the new TFT and the conventional TFT. W/L=20/10 um

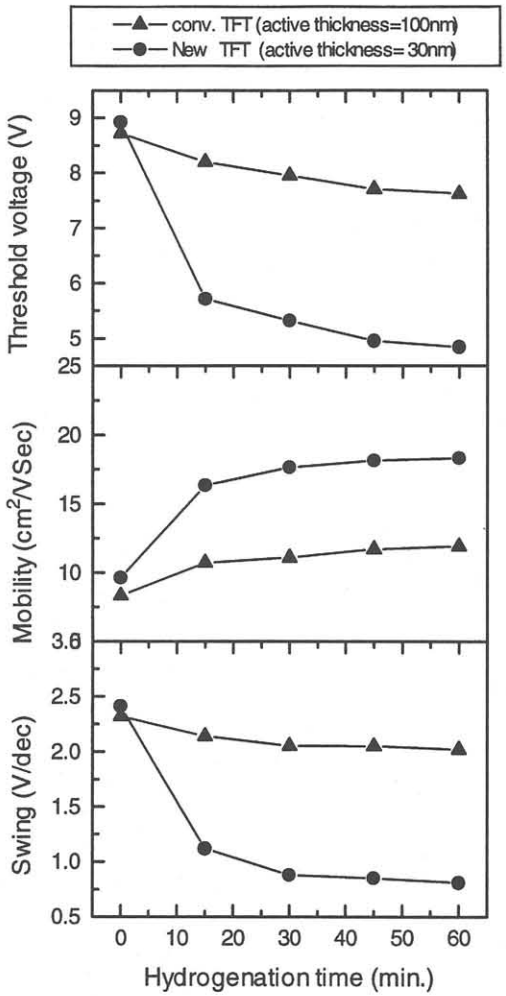


Fig. 4 The variation of the device characteristics ( $V_{th}$, $\mu_{fet}$, subthreshold slope) with the hydrogenation time for the new device and the conventional device.


## ACKNOWLEDGMENT

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