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A Novel High Density EEPROM Cells Using Poly-Gate Hole (POLE) Structure Suitable for Low Power Applications

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A novel high density EEPROM cell technology is proposed. The new cell structure utilizing **PO**ly-gate ho**LE**(POLE) can reduce channel length with 9 nm gate oxide and eliminate huge substrate current (Isub) induced by band-to-band tunneling. The resultant Isub can be reduced 2 orders as compared with conventional Flash cells by isolating a charge transfer region from a cell channel region . This technology is promising for the future generations with CMOS embedded process. A 36 um2 cell size which is 20 % smaller than FLOTOX with 0.6 um design rule can be realized.

1 Introduction

An EEPROM is of great use in a broad applications field, for example IC card, RF card, Phone, Pager, MCUs, and ASICs. Therefore, CMOS logic based embedded EEPROM LSIs [1), 2)] are strongly required and they should operate on a single power supply voltage (< 1.8 V) as well as low power consumption for battery use. A cell technology reduce write / erase current [3)] to meet on-chip charge pumping and realize a large number of W/E cycling (> 1 million) with byte W/E functions in the key issue. The FLOTOX cell [4)] has been historically used, but the shrink rate is too poor compared with CMOS's. On the other hand, channel hot electron write based Flash cells consume much power.

2 New cell structure

The new cell structure as shown in Fig. 1 has a memory transistor (MT) and select transistor (ST) in series for Fowler - Nordheim (FN) tunneling byte write/erase operations. A uniform thin oxide of 9 nm on the channel , source and drain regions of MT can reduce Vpp below 18 V during FN tunneling in W/E. The floating gate , the control gate and the gate poly-hole are formed by self-aligned process. This is much simpler compared with FLOTOX process.

The poly gate hole has an important role to separate the charge transfer region from the channel , as well as to reduce substrate current. The self-aligned N- diffused layer which can be realized in a FLOTOX is formed under POLE region with the control gate as an ion implantation mask. The channel length can be reduced by using the thin gate oxide and determined from POLE edge to MT N+ edge. A 36 um2 cell size with 0.6 um rules without any additional process steps for FLOTOX can be realized. The cell size is 20 % smaller than that of FLOTOX cell.

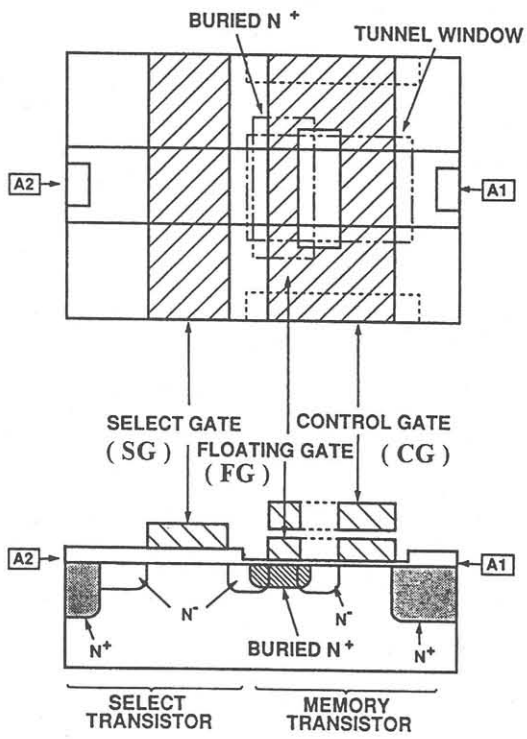
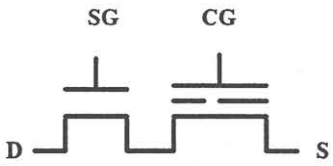


Figure 1 : Plan view and cross section of the new EEPROM cell.

Figure 2 summarizes the operation models. In the erase mode, FN current is injected from the channel, source and drain to the floating gate (FG). In the write mode, FN current flows from the FG to the buried N+ of the MT drain. Erased Vt and written Vt are positive and negative, respectively. In the read mode, 1V is applied to the drain with the control gate grounded to prevent a read disturb.



	D	SG	CG	S
ERASE	0	Vpp	Vpp	0
WRITE	Vpp	Vpp	0	OPEN
READ	1	Vcc	0	0

Figure 2 : Write, erase and read operations of the new cell.

3 Isub reducing model and results

Figure 3 shows how Isub is reduced in the new cell. Generally in the write operation, the band-to-band tunneling hole current continues to flow from the N+ edge to the substrate. In this cell, however, the hole current dose not flow out of the edge of the buried N+ diffused layer even if Vpp is applied to the drain. Because the FG does not exist over the edge point. Therefore, generated cold holes during the write are kept and saturate just under the poly gate region. The surrounded N- prevents to flow out them. Therefore, POLE acts as the hole stopper.

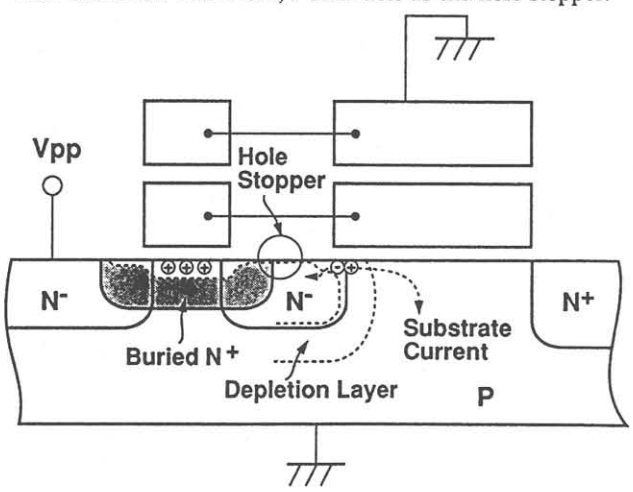


Figure 3 : POLE structure and hole-stopper in the new cell.

In addition, a band-to-band tunneling current at the N- edge of channel region is also greatly reduced, because N- concentration can be optimized independently from the buried N+ doping. The maximum spacing L between the gate edge and the buried N+ is found to be 0.4 um for suppressing Isub as shown in Fig. 4, which is substantially less than the size of POLE.

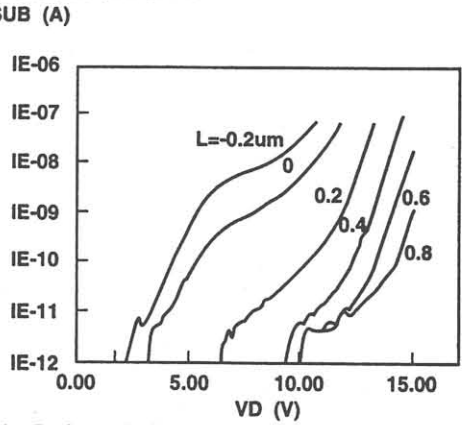


Figure 4 : Isub vs. Vd as a parameter of N- length in the contacted FG cell at Vfg= -4 V.

Figures 5 (a) and (b) show Isub and floating gate current (Ifg) of a contacted floating gate cell for conventional Flash and the new cell, respectively.

Allowable supply current per cell with a reasonable pumping circuit size is the Max. Isub (20 nA). Min. Ifg is the required tunneling current (100 pA) to write and erase. As shown in Fig. 5 (a), in a channel hot electron write Flash cell, Isub is almost 2 orders of magnitude larger than Ifg. In POLE cell, Ifg is almost the same as Isub (Fig. 5(b)). This means that the proposed POLE structure can effectively suppress Isub induced by band-to-band tunneling. It can provide a large margin in designing LSIs.

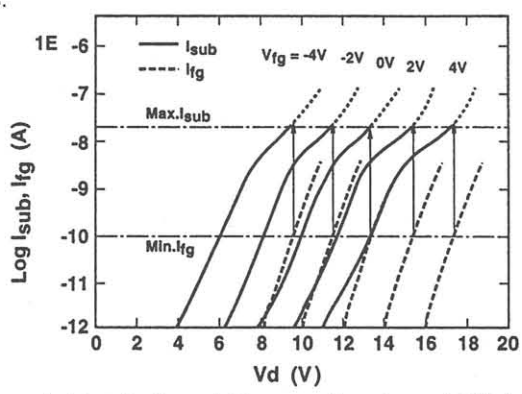


Figure 5 (a) : Isub and Ifg as a function of Vd in the conventional Flash cell.

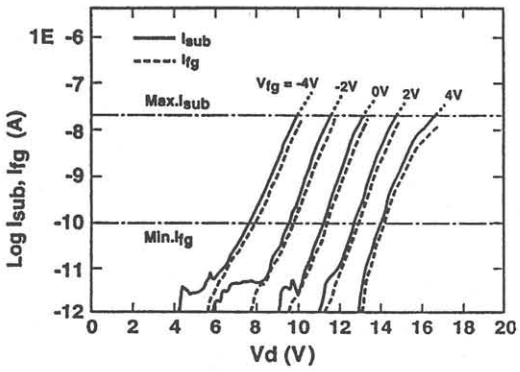


Figure 5 (b) : Isub and Ifg in the new cell.

4 Cell characteristics and reliability

Figure 6 shows write, erase and read characteristics of the new cell. Substantial margin in write, erase and read operations are confirmed.

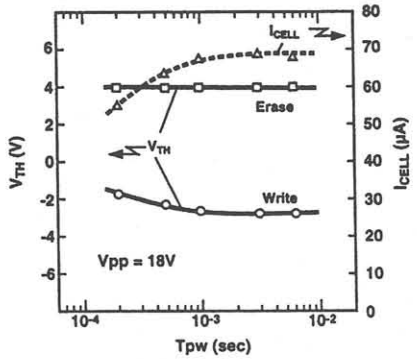


Figure 6 : Write, erase and read current characteristics.

W/E endurance characteristics is shown in Fig. 7. Even 1 million cycles, no memory window narrowing and cell channel current Icell above 60 uA are confirmed.

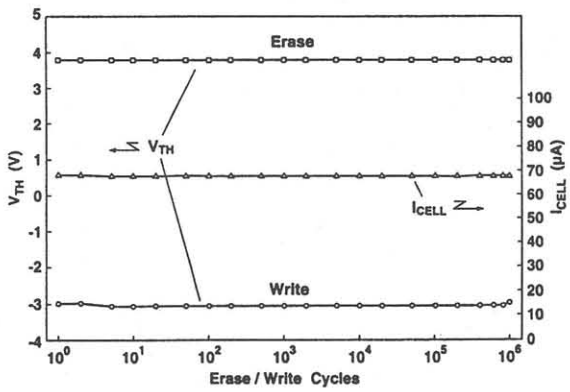


Figure 7 : W/E endurance characteristics (Vpp : 18 V, Tpw : 2 ms)

Data retention characteristics is shown in Fig. 8. The activation energy is 1.07 eV, which is comparable to that of FLOTOX cells. It is enough to ensure the data retention during 10 years at 90 ℃.

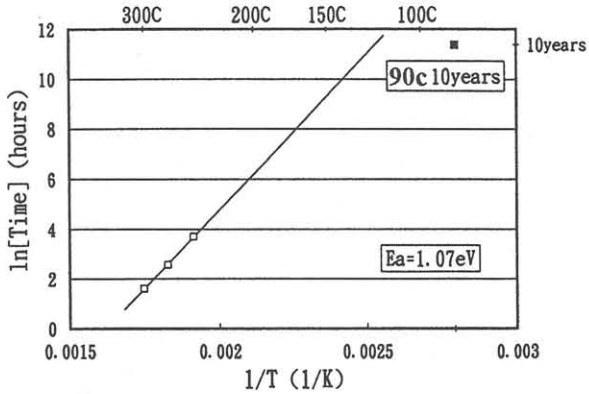


Figure 8 : Data retention characteristics.

5 Conclusions

Achieved performance using POLE cell structure is confirmed as follows :

(1) To have hole stopper in the cell, Isub (band-to-band tunneling current) at write operation, can be reduced 2 orders compared with conventional Flash cells. It is possible to realize charge pumping operations on chip and low power consumption EEPROMs.

(2) A 36 um2 cell size with 0.6 um rules without any additional process steps for FLOTOX cells can be realized. The cell size is 20 % smaller than that of FLOTOX cell. It is promising for the future generation with CMOS embedded process.

(3) For the reliability, 1 million cycling endurance and 10 years data retention at 90℃ have been achieved.

6 References

1) M. Takebuchi et al. IEEE CICC proceedings. p. 9.6.1, 1992.

2) T. Fujimoto et al. IEEE 12th NVSMW, 1993 , Monterey.

3) J. Noda et al. IEEE 13th NVSMW, 1994, Monterey.

4) A. Kolodny et al., IEEE Trans. **ED**-33, vol.6, p.128 , June, 1986