Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 64-66

Comparison of Over Erase Susceptibility and Cycling Reliability between Channel Erase and Bitline Erase in Flash EEPROM

Jen-Tai Hsu and Stuart Shumway

Memory Product Division, National Semiconductor Corporation
Mail Stop 5006
3333 West 9000 South, West Jordan, UT 84088-8838, USA

In this paper, we report for the first time the comparison of over erase susceptibility between channel erase and bitline erase in flash memory. It is shown that due to larger tunnel area in channel erase, channel erase is more susceptible to over erase than bitline erase. In addition, program/erase cycling data shows that although cycling degradation was lower in channel erase than bitline erase due to less hot-hole generation up to 10^5 cycles, channel erase degrades faster and exceeds the degradation in bitline erase between 10^5 and 10^6 cycles.

1. Introduction

The threshold voltage after erase (Vte) of a flash array usually shows a main normal distribution with tail distributions. To ensure that the maximum Vte to be identified as "erased", the lower tail bits can go into depletion causing leaky column array failure or erratic erase behavior which impacts on cycling reliability [1].

Channel erase is considered capable of alleviating the tunnel oxide degradation from cycling stress compared to Bitline erase due to its less hot hole generation and trapping in the oxide.

In this paper, we report for the first time the comparison of over erase susceptibility between channel erase and bitline erase in flash memory. It is shown that due to larger tunnel area in channel erase, channel erase is more susceptible to over erase than bitline erase. This difference can become more significant as the array density increases. Even with the implementation of self-convergence scheme to avoid over-erasing the cells [2,3,4], channel erase still shows larger distribution of erased Vt compared to bitline erase. In addition, program/erase cycling data shows that although cycling degradation was lower in channel erase than bitline erase due to less hot-hole generation up to 10^5 cycles, channel erase degrades faster and exceeds the degradation in bitline erase between 10^5 and 10^6 cycles.

2. Experimental

Nor Virtual Ground (NVG) Flash memory cells [5] were used in this study. The test structure consists of 88 cells in a mini-array with 0.65μm drawn L and 11nm tunnel oxide. Program of the cells were done by 12V on gate and 6V on drain with duration of 10μs. Channel erase (CE) was performed by applying -15V on the gate and 3V on the substrate with bitlines floating. Bitline erase (BE) was done by -15V on the gate and 3V on the bitlines while grounding the substrate. For comparison, the erase time in both cases is controlled to achieve the same median erased Vt in the distribution. Additional programming-back step (Pgmback) for convergence was done by 17V on the gate while grounding both bitlines and substrate. The voltage conditions for above four different operating modes are shown in Table 1. The cell characterization is performed with an HP4156A Precision Semiconductor Parameter Analyzer.

3. Investigation of Over Erase Susceptibility

Channel erase and bitline erase were implemented on the same samples after identical program step. In Fig.1, bitline erased Vt (Vte,bit) are plotted against channel erased Vt (Vte,ch) for each over erased cell. Region II (Vte,ch<0, Vte,bit>0) corresponds to those cells that were erased to depletion by channel erase but to normal level by bitline erase. On the contrary, Region IV (Vte,ch>0, Vte,bit<0) corresponds to the cells that were erased to depletion by bitline erase

but works normal with channel erase. Region III shows the cells that were erased to depletion for both erase methods. Region II has more than three times of over erased cells than Region IV or III. Fig.2 shows typical cumulative erased Vt distribution with tail bits going into depletion by channel erase but not by bitline erase We believe that all the over erased cells are due to enhanced tunneling sites because channel erase uses larger tunnel area than bitline erase.

It has been shown that an additional programming-back step can help to suppress erased Vt distribution [2]. In order to apply this two step erase scheme, the erased Vt in the first step should be approximately 1V below the target Vt after applying the second programming-back step. In this work, we also investigated the erased Vt distribution with additional programming-back step (1sec) following the same erase time (1sec) to suppress Vt distribution. As shown in Fig.3, bitline erase has much tighter distribution (1.5V) compared to channel erase (2.9V). The additional programming-back step suppresses the tail distribution very efficiently after bitline erase, but not after channel erase. This results suggests that the enhanced tunneling site probably results from traps but not thin spots or defects due to the asymmetric tunneling behavior.

4. Program/Erase Cycling Results

We compared the cycling reliability for channel and bitline erase in Fig. 4. Channel erase exhibits better reliability up to 10^5 cycles as expected. However, from 10^5 to 10^6 cycles, bitline erase shows saturation in degradation and demonstrates better reliability than channel erase. This result can be attributed to two factors: first, we use negative gate voltage and low bitline voltage in bitline erase to reduce hot hole generation; secondly, in the bitline erase, the tunneling area is smaller so that the degradation can saturate faster than the larger tunnel area in channel erase. The results of P/E cycling on over erased cell with additional programming-back step is shown in Fig.5. The difference between the erased Vt and the programming-back Vt decreases with cycles due to continuous degradation in tunnel oxide.

The cycling result without tunnel oxide breakdown suggests that the over erase of the cell is not likely due to thin spots or oxide defects. Most probably it is due to hole traps generated from plasma damage. The traps can enhance tunneling initially, but tends to lose its effectiveness as they are gradually filled by holes with P/E cycling.

5. Conclusion

Although commonly channel erase is considered to be better for cycling reliability than bitline erase, this study demonstrates that it is more vulnerable for over erase due to its larger tunneling area. Bitline erase with negative gate voltage and small bitline voltage showed better cycling reliability than channel erase after 10^5 cycles although it degraded faster up to 10^5 cycles. The cycling results on over erased cell suggests that the over erase is caused by oxide traps instead of thin spots or defects.

References

1) T. C. Ong, A. Fazio, N. Mielke, S. Pan, N. Righos, G. Atwood, and S. Li, VLSI Symposium, 1993, p.83.

2) K. Oyama, H. Shirai, N. Kanamori, K. Saitoh, Y.S. Hisamune, and T. Okazawa, IEDM, 1992, p.607.

3) S. Yamada, T. Suzuki, E. Obi, M. Oshikiri, K. Naruke, and M. Wada, IEDM, 1991, p.307.

4) K. Yoshikawa, S. Yamada, J. Miyamoto, T. Suzuki, M. Oshikiri, E. Obi, Y. Hiura, K. Yamada, Y. Ohshima, and S. Atsumi, IEDM, 1992, p. 595.

5) A. Bergemont, H. Haggag, L. Anderson, E. Shacham, G. Wolstenholme, IEDM, 1993, p.15.

Program/Erase Conditions

	VG	VD	VS	Vsub	Time
Program	12V	6V	0V	0V	10 us
CE	-15V	float	float	3V	1 s
BE	-15V	3V	3V	0V	0.1 s
Pgmback	17V	0V	0V	0V	1 s

Table 1. Voltage conditions for four different operating modes.

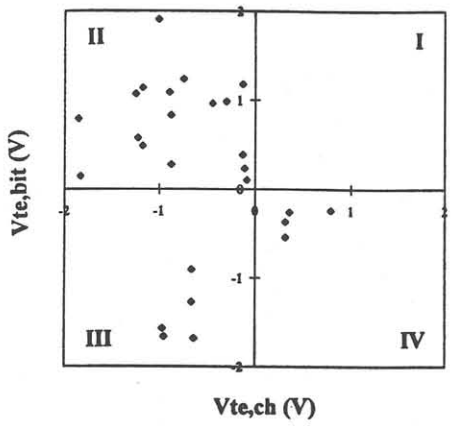

Figure 1. Channel Erased Vt (Vte, ch) versus Bitline erased Vt (Vte, bit) for all the over erased cells. Each point represents one cell.

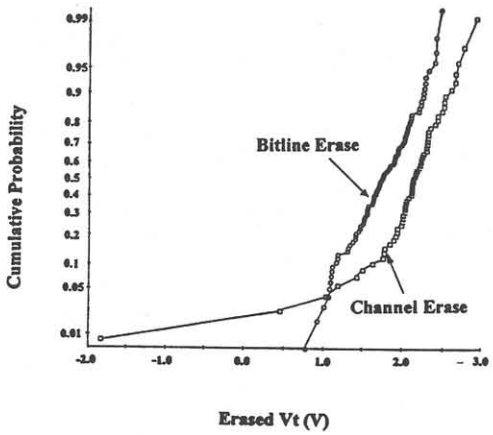

Figure 2. Typical cumulative erased Vt distribution by channel erase and bitline erase.

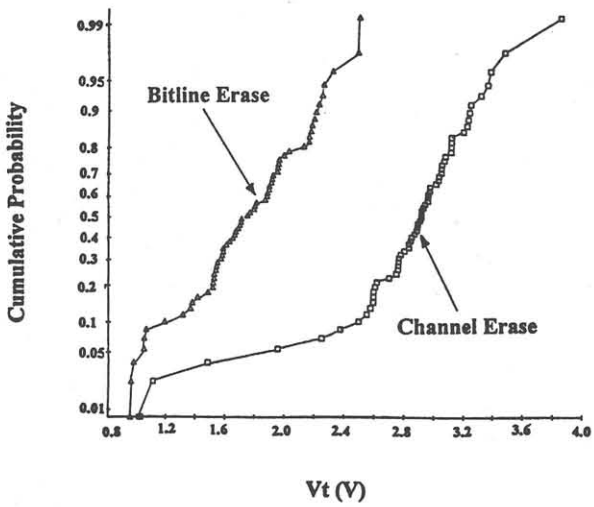

Figure 3. Cumulative Vt distribution after additional programming-back step for channel and bitline erased cells.

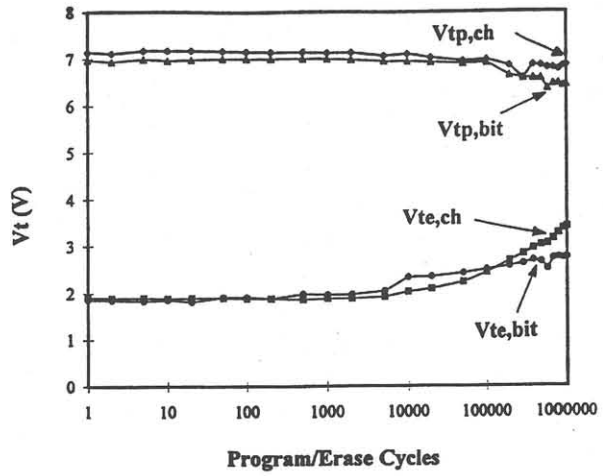

Figure 4. Program/Erase cycling for channel and bitline erase.

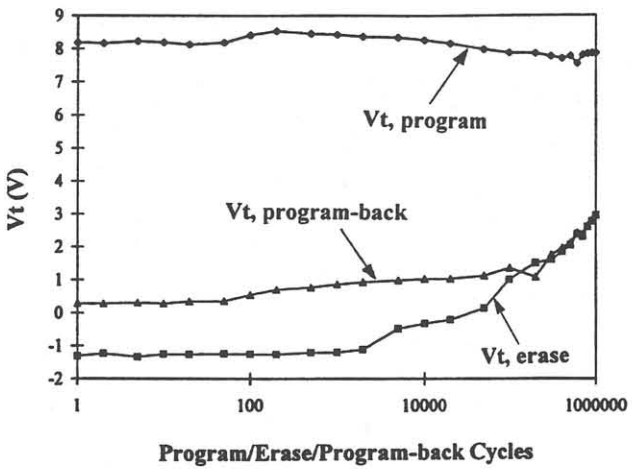

Figure 5. Program/Erase cycling for an over erased cell with additional programming-back step.