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Low-Voltage and Power CMOS Technology

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This paper describes that lowering threshold voltage, shortening gate length, thinning gate oxide and reduction in parasitic capacitance are indispensable for CMOS devices with low-voltage supply, in order to keep consistency between circuit performance and power dissipation, based upon theoretical understanding. Furthermore, the standby power reduction circuit has been proposed to keep standby power low with expected improvement in circuit performance by continuous device scaling even at low-voltage.

1. Introduction

The basic scaling theory suggested that scaling MOS device has provided significant reduction in power dissipation per a circuit and improvement in circuit performance as well as increase in packing density [1]. Most of LSIs have actually enjoyed all of advantages by using continuous scaling down of MOS devices for these two decades with gradual shift to CMOS technology. However, a severe problem concerning increase in power dissipation has been actualized owing to higher frequency and packing density required from the semiconductor market even in the CMOS LSI. This problem is beyond the level which is achievable by scaling down of MOS devices with constant voltage or innovation of packaging technology. Moreover, a strong demand for battery-operated systems with moderate performance should accelerate development of low-power CMOS LSI [2]. While system and algorithm innovation is most effective for reduction in power dissipation, in order to emphasize its effectiveness, device engineering and process development are necessary.

In view of the above considerations, this paper describes device technologies for low-power CMOS devices at low-voltage operation. Based upon theoretical analysis of the CMOS circuits behavior, it has been clarified that reduction in parasitic capacitance, lowering threshold voltage and selective scaling concept are important to achieve low-power CMOS devices. Moreover, an example is presented to realize the low standby CMOS circuits without sacrificing performance.

2. Power Dissipation of CMOS LSI

It is well accepted that power dissipation in the CMOS LSI can be given by the following two equations.

$$P_{operation} = \alpha \cdot C_{load} \cdot V_{load} \cdot V_{DD} \cdot n \cdot f \approx \alpha \cdot C_{load} \cdot V_{DD}^{2} \cdot n \cdot f \qquad (1)$$

$$P_S = I_{leak} \cdot V_{DD} \qquad (2),$$

where $P_{operation}$ is power consumption during operation, P_S is the average static power, α is activation rate, n is the number of the logic gate, C_{load} is the switching capacitance per one gate such as gate capacitance and wiring capacitance, V_{load} is the signal swing and V_{DD} is operating voltage, f is a repetition frequency, and I_{leak} is the leakage current in the LSI caused by subthreshold and junction leakage. Although transient current between nMOSFET and pMOSFET exists, this value can be neglected during operation. It has been confirmed that experimental results in Fig. 1 support accuracy in Eqs. 1 and 2.

Therefore, lowering operating voltage without sacrificing circuit performance and minimizing parasitic capacitance are key issues from the device point of view, although α, n, and f terms are improved by using advanced system/algorithm and circuit improvement [3]. Therefore, it is significant for low-power CMOS devices to understand the relationship between operating voltage and the circuit delay.

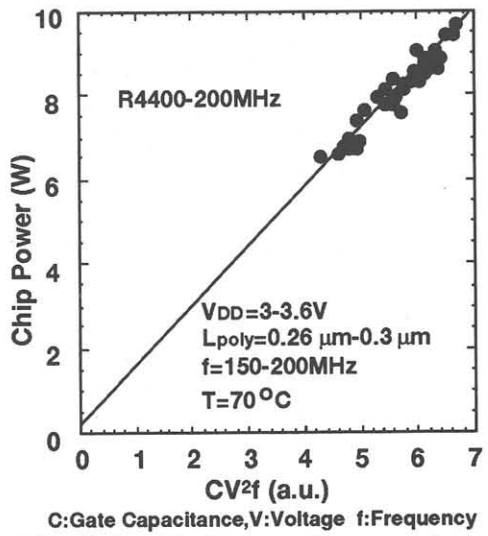

Fig. 1 The relationship between the power dissipation of the microprocessor and normalized CV²f in various ploy gate length from 0.26μm to 0.3μm with range from 150MHz to 200MHz under 3.0-3.6V operation. The intercept value in the power axis should mean standby power.

3. CMOS Circuit Performance at Low-Voltage

A typical delay time versus voltage curve for a CMOS device is log-log plotted in Fig. 2. As shown in Fig. 2, the fall time initially decreases with increasing power-supply voltage. On the other hand, when V_{DD} becomes higher than the critical voltage Vc, saturation of improvement in circuit delay begins to occur, and finally, the delay is independent of the power-supply voltage. This is because the delay time of CMOS devices consists of two intervals; constant τ_1 (technology dependent) and τ_2 which is inversely proportional to V_{DD} [4]. At lower voltage less than Vc, dependence of the delay on operating voltage is large, since the total delay time is dominated by τ_2. Accordingly, operating voltage should be higher than the Vc to become insensitive to operating voltage. The critical voltage Vc can be expressed as

$$V_c = 0.87 E_c L_{eff} + V_{th} \qquad (3),$$

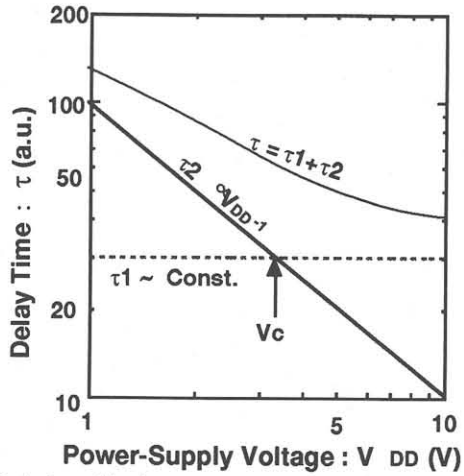

Fig. 2 Relationship between power-supply voltage and the delay time. The Vc is defined as the intersection point between τ1 and τ2 curves.

where Ec is the critical electric field at which carrier velocity is saturated, Leff is the MOSFET's effective channel length, Vth is the threshold voltage of MOSFET [5]. As clearly indicated in Eq. 3, shortening of the effective channel length and lowering threshold voltage are essential in order to reduce the Vc as low as possible.

Since the gate delay increases rapidly because of drastic reduction of MOSFET's current level as the threshold voltage approaches one half of VDD, as shown in Fig. 3, the threshold voltage should be less than 20% of power-supply voltage [6].

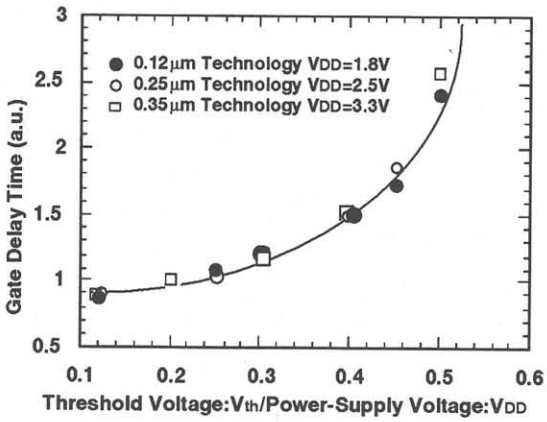

Fig. 3 The gate delay time of the CMOS inverter with F/O=3 as a function of the ratio of the threshold voltage to power-supply voltage.

On the other hand, the subthreshold leakage current at VG=0 is inevitably increased, when the threshold voltage is lowered as far as possible from the viewpoint of circuit performance. This is because it is difficult to improve the subthreshold slope by adjusting device parameters. Accordingly, it is necessary to introduce circuit technique combined with advanced CMOS technology to have consistency between high performance and low standby power as discussed later.

Figure 4 shows the dependence of the gate delay time of CMOS circuits and the power dissipation per a gate with F/O=3 and 2mm Al line on the power-supply voltage for 0.2μm gate electrode with parameters of the threshold voltage, gate oxide thickness and the effective channel length. While the delay-voltage curves are sensitive to various parameters, power dissipation per gate is not so sensitive. Therefore, for a given circuit performance (frequency), obtained power dissipation is strongly dependent upon various device parameters. For example, if 300ps/stage is given as a criterion of performance, standard CMOS process requires 2V operation, and its power dissipation is 1.6pW/cycle. However, when the threshold voltage is 0.25V, gate oxide thickness is reduced to 4.5nm and effective channel length is lowered to 0.12μm, required operating voltage is reduced to be 1.2V, and thus, the power dissipation is 0.6pW/cycle. As a result, saving power by about 60% can be realized by choosing device parameters which is specific for low-voltage operation. Moreover, Fig. 4 indicates that thinning gate oxide thickness is also indispensable for low-power CMOS in order to keep channel current drivability which is critical for the long metal line drive [7].

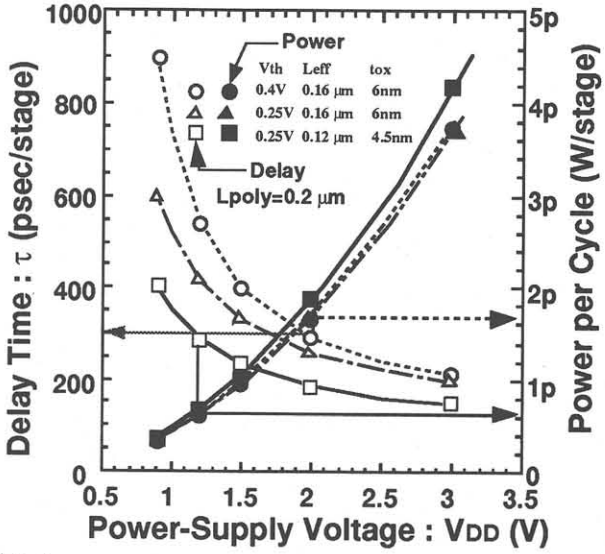

Fig. 4
Gate delay and power dissipation versus operating voltage for CMOS inverters (F/O=3) with 2mm Al. Each arrow indicates attainable power dissipation for a given 0.3ns gate delay.

4. Reduction of Parasitic Capacitance

The Eq.1 also teaches us that parasitic capacitance such as junction capacitance, gate capacitance and wiring capacitance play an important role in power dissipation. Since gate oxide thickness is determined considering trade-off between MOSFET current drivability and gate capacitance, it cannot be decided only from the power point of view. The junction capacitance is inversely proportional to the square root of the drain voltage, while the gate capacitance and the wiring capacitance are independent of operating voltage. Therefore, the junction capacitance is naturally increased as operating voltage is decreased. Accordingly, reduction of the junction capacitance is a key issue for achieving high circuit performance at low-voltage operation. Various approaches to minimize the junction capacitance are the SOI device [8], substrate engineering such as CMOS-SJET technology [9] and Shallow Trench Isolation (STI) structure in Fig. 5 [10].

The only way to offset the increase in wiring capacitance during scaling downwards is reducing the dielectric

constant in the interlayer dielectric. It has been reported that a relative dielectric constant of 3.4 can be achieved by incorporating fluorine during deposition process [11]. This technology makes it possible to decrease power dissipation as well as achieve higher performance.

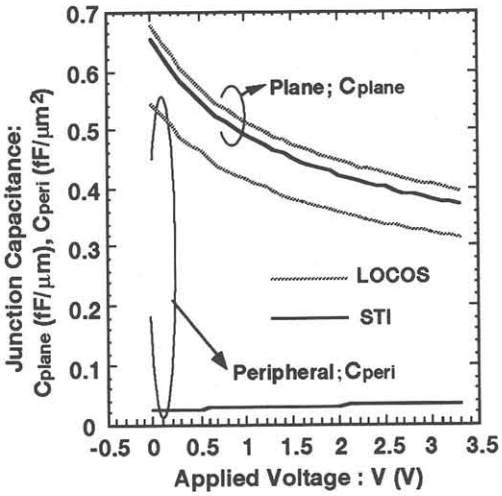

Fig. 5
Comparison of junction capacitance between STI and LOCOS isolation.

5. Standby Power

The only drawback by choosing low threshold voltage, as discussed in the previous section, is the increase in standby power dissipation. However, if the threshold voltage is controlled from the subthreshold leakage point of view, obtained results cannot suffice expected circuit performance. Therefore, the steeper subthreshold slope is desirable for reduction of the threshold voltage with maintaining low subthreshold leakage. Even if the SOI device and substrate engineering are introduced [12], the lower limit of subthreshold slope is about 60mV/decade at room temperature owing to its physical limit. Therefore these technologies are not necessarily eternal solutions to reduce subthreshold leakage in the future. On the other hand, low-temperature CMOS (LT-CMOS) can provide very steep slope with other major advantages [13]. However, LT-CMOS is not practically available in the commercial market because of difficulty associated with economical refrigeration system and special packaging technology required for low-temperature operation.

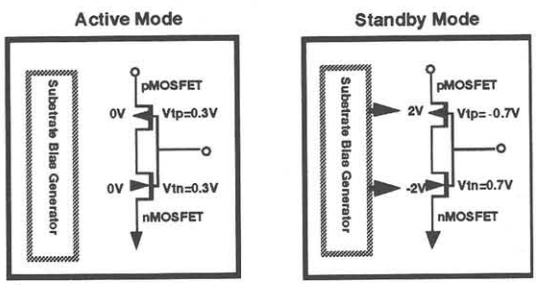

Fig. 6
Concept of Standby Power Reduction (SPR) circuit.

New circuit concept in Fig. 6 has been proposed to dissolve the dilemma as described above [14]. The main idea of the standby power reduction (SPR) is that a substrate bias in a standby mode to increase the threshold voltage and to decrease subthreshold leakage current. In an active mode, the substrate bias is 0V, and thus the threshold voltage is enough low to assure high-speed operation. It has been verified that about 3-4 orders of magnitude of standby current can be reduced by this technique in the experiment, compared with the conventional CMOS circuit scheme.

6. Conclusion

This paper has discussed device technologies of low-power CMOS devices. In order to save the power dissipation in CMOS LSI, reduction in power-supply voltage is very critical. It is essential to lower the threshold voltage, make gate oxide thin and shorten effective channel gate length corresponding to low-voltage operation compared with the standard CMOS device. Moreover, reduction of parasitic capacitance is indispensable for the low-power CMOS device to achieve high-speed operation as expected from MOS device scaling. While several device technologies exist to lower subthreshold leakage, adjustment the threshold voltage in standby mode by using circuit technology can lead to the CMOS device with consistency with low threshold voltage in an active mode.

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