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A New Triple-Well Process to Accomplish a Lower Vth and a Low Cost for Low Power-Supply Voltage VLSI

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We have developed a new triple-well method to accomplish a MOSFET with a lower Vth and a low cost. The new triple-well with a retrograde P- and isolated-Pwell is fabricated by two lithography steps using only the conventional ion-implantation equipment. The cost of the new triple-well is lower than MeV triple-well in the lower production volume. Good latch-up immunity is obtained without using the high energy ion-implantation equipment. An experiment on 0.35 μ m DRAM shows a good performance.

1. Introduction

High speed operation at low power-supply voltages is required for VLSI technology. On the other hand simple processing is necessary for the low cost devices. These two topics are very dependant on the well process(1-4). In the conventional diffused triple-well, if ion-implantation for the n- and p-MOSFET's V th adjustment is carried out without a mask (the blanket ion-implantation for Vth adjustment), at least three lithography steps for the ion-implantation exist before the gate oxidation. These are for the Nwell formation, P- and isolated-Pwell and n-channel stop. In the conventional diffused triple-well formed by the three lithography steps, the concentration of each well is designed as follows.

1) The minimum dosage for the diffused Nwell formation is determined to suppress the leakage current of the parasitic p-ch field transistor.

2) The minimum dosage for the diffused P- and isolated-Pwell is determined to isolate the n^+ (in the isolated-Pwell) from the Nwell.

These two limitations cause the concentrations of both well to be higher. These lead to higher n- and p-MOSFET's Vth. MOSFETs with high Vth has a disadvantage in high speed operation at low power-supply voltages. Ultimately, more lithography steps are required to get a lower V th. One effective approach to solve this problem is to adopt the retrograde well using high energy ion-implantation (acceleration energy more than 200 keV). The V th of a MOSFET with a retrograde triple-well is lower than that of the conventional diffused triple-well because of retrograde's lower surface concentration. The ion-implantation for the retrograde Nwell in the triple-well requires more than 1 MeV phosphorus ions. However the high energy ion-implantation equipments covering more than 1 MeV are still expensive, so the cost of the retrograde triple-well using high energy is high in the lower production volume (Fig.1(b)) and adopting only one high energy equipment at each factory is fatal in the machine trouble.

We have developed the new triple-well process using only the conventional ion-implantation equipment (less than 200 keV). The MOSFET's V th of the new triple-well having the retrograde P- and isolated-Pwell is lower than that of the conventional diffused triple-well. Though the MeV triple-well also can achieve the lower Vth, the cost of the new triple-well is lower than MeV triple-well in the lower production volume (Fig.1(b)). The new well process is safe in the machine trouble for using only the conventional ion-implantation equipment. The experiment on 0.35 μ m DRAM shows a good performance.

2. Fabrication process

The new triple-well was fabricated by the following procedure. The 180 keV phosphorus ions for the Nwell formation were implanted with a dose of 1.3×10^{13} cm^{-2} into P-type substrate after the isolation patterning (Fig.2(a)).

The Nwell drive-in anneal and the field oxidation were done (Fig.2(b)).

The 180 keV boron ions were implanted with a dose of 1.5×10^{13} cm^{-2} in order to form the retrograde P- and isolated-Pwell at the same time. Next, without stripping the resist the 100 keV boron ions for the n-channel stop were implanted with a dose of 3.5×10^{12} cm^{-2}(Fig.2(c)). The blanket ion-implantation for the n-and p-MOSFET's Vth adjustment was carried out (Fig.2(d)).

The n- and p-MOSFET were then fabricated in the conventional process. The triple-well process described above uses only two masks for the ion-implantation with conventional ion-implantation equipment.

Figure.1(a) shows a comparison of the fabrication steps between the conventional diffused triple-well, the MeV triple-well and the new triple-well. We don't discuss about the MeV triple-well in here. The number of masks in the new triple-well has decreased to two in comparison with conventional well, because the ion-implantation of Pwell and isolated-Pwell formation is performed after the field oxidation with the mask of the n-channel stop. The total drive-in anneal time is also shortened by this method.

Figure.3 shows the impurity profiles by SIMS in the isolated-Pwell and Nwell region after the V th adjustment implantation.

3. Results and discussion

Figure.4 shows the breakdown voltage between the n^+ (in the isolated-Pwell) and Nwell as a function of the n^+ region to Nwell edge. The results show that the breakdown voltage of the new well is slightly better than the conventional well as the spacing decreases.

Figure.5 shows the n- and p-MOSFET's V th as a function of the dosage of the blanket ion-implantation. In comparison with the conventional diffused P- and isolated-Pwell, the threshold voltages of the new well are lower by about 0.15 V in the Pwell, an about 0.2V in the isolated-Pwell for the same dosage because of the lower surface concentration. The p-MOSFET's V th doesn't change because of using the diffused Nwell, but the n-MOSFET's Vth is low enough to increase the n- and p-MOSFET's blanket V th adjustment. As a result, the lower n- and p-MOSFET's V th can be obtained.

The latch-up immunity of CMOS has been evaluated by measuring the switching current. Figure.6(a) and 6(b) show the switching currents as a function of n^+ to p^+ spacing. Compared with conventional diffused well, the switching current of the new triple-well were improved by about 25% for the Nwell / Pwell and more than 150 % for the Nwell / isolated-Pwell. These are due to the reduction of the current gain of the parasitic bipolar transistors and the decrease of P- and isolated-Pwell resistivity in the new triple-well structure. The above results indicate the higher packing density VLSI is available using this process.

The junction capacitance of the new triple-well is about 4% larger than the conventional well (Fig.7), but there are no speed delay on the 0.35 μm DRAM.

We also checked refresh characteristics to evaluate the defects especially locally existing one (Fig.8). The result shows that the refresh worst time of the new triple-well is almost same as the conventional well and the peak time of new well is slightly better.

4. Conclusions

The new triple-well with a retrograde P- and isolated-Pwell is fabricated by only two mask steps using the conventional ion-implantation equipment. A lower V th MOSFET is available because of the retrograde profile, even if the blanket Vth adjustment is adopted. The reduction in the cost is also achieved. Good latch-up immunity is obtained without using high energy ion-implantation equipment. The experiment on 0.35 μm DRAM shows a good performance.

5. Acknowledgment

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6. References

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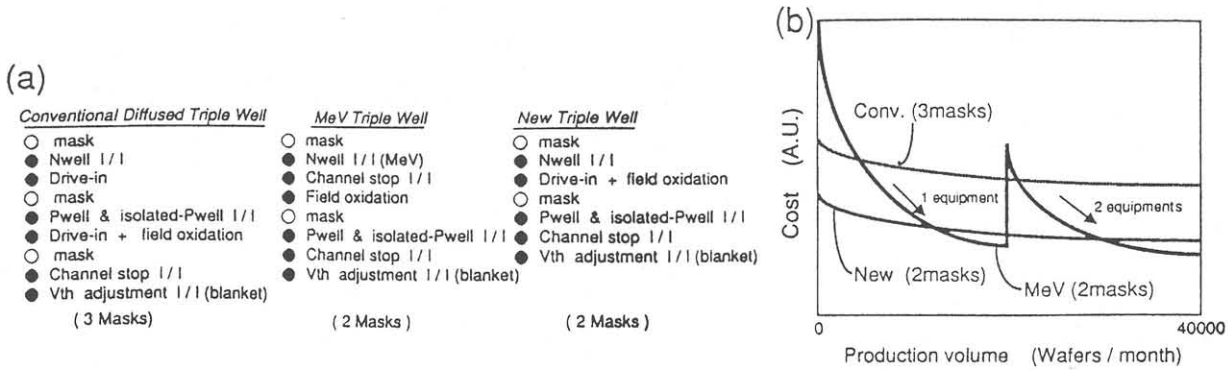

Fig.1 (a) Comparison of the fabrication process between the conventional diffused triple-well(3 masks), the MeV triple-well(2 masks) and the new triple-well(2 masks). (b) Cost as a function of the production volume.

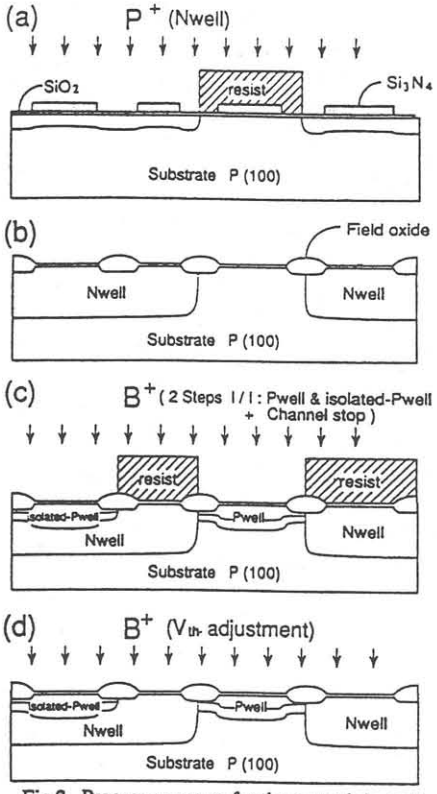

Fig.2 Process sequence for the new triple-well.

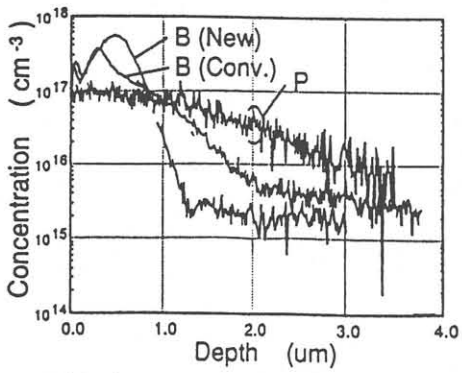

Fig.3 Impurity depth profiles by SIMS after the V_{th} adjustment implantation.

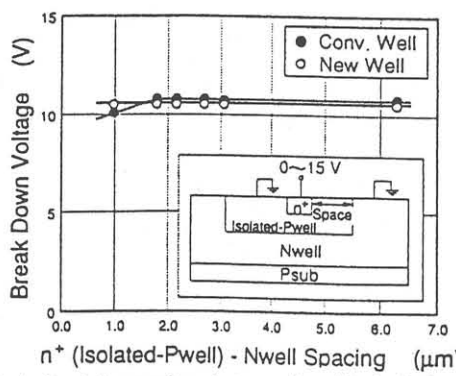

Fig.4 Breakdown voltage between the n^+ in the isolated-Pwell and Nwell as a function of the spacing from the n^+ region to the Nwell edge, where threshold leakage current is 1nA.

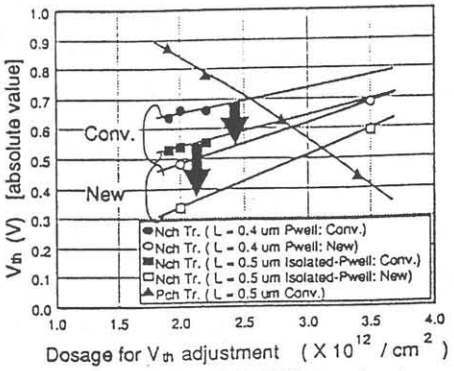

Fig.5 V_{th} for n- and p-MOSFETs as a function of blanket ion-implantation dosage.

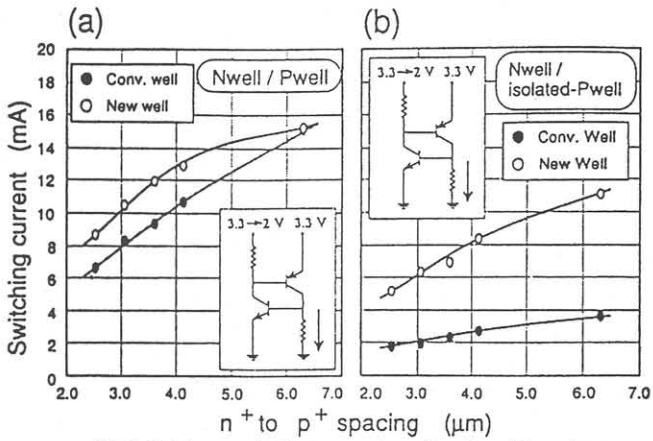

Fig.6 Latch-up switching current as a function of the n^+ to p^+ spacing at the triggering condition due to forward biased p^+ to Nwell junction.

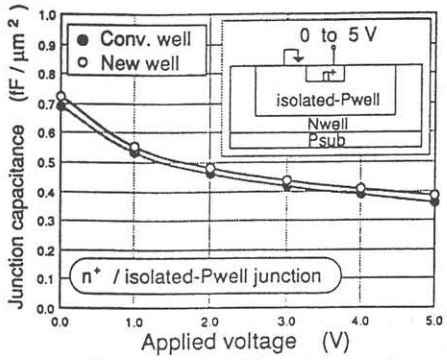

Fig.7 n^+ / isolated-Pwell junction capacitance as a function of applied voltage.

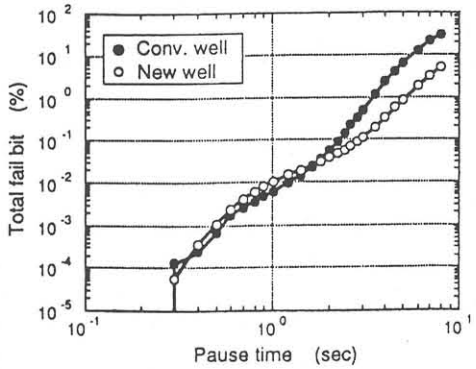

Fig.8 Comparison of the refresh characteristics between the conventional diffused triple-well and the new triple-well at 85℃ for the typical chip of 0.35 μ m DRAM.