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Impact of Nitrogen Implantation on Highly Reliable Sub-Quarter Micron LDD MOSFETs

S. Shimizu, T. Kuroi, S. Kusunoki, Y. Okumura, M. Inuishi and T. Hirao

ULSI Laboratory, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo 664 JAPAN

We present the highly reliable sub-quarter micron LDD N-MOSFETs, employing nitrogen implantation into the side-wall SiO_2. This novel structure can effectively reduce the hot carrier degradation for LDD N-MOSFETs. The improvement of hot carrier degradation should be due to the segregation of nitrogen at the interface between the substrate and the side-wall SiO_2, thereby reducing the generation of interface states at the drain edges. Therefore we can realize the highly reliable sub-quarter micron LDD N-MOSFETs without the increase of gate resistance and the depletion of gate polysilicon.

1. INTRODUCTION

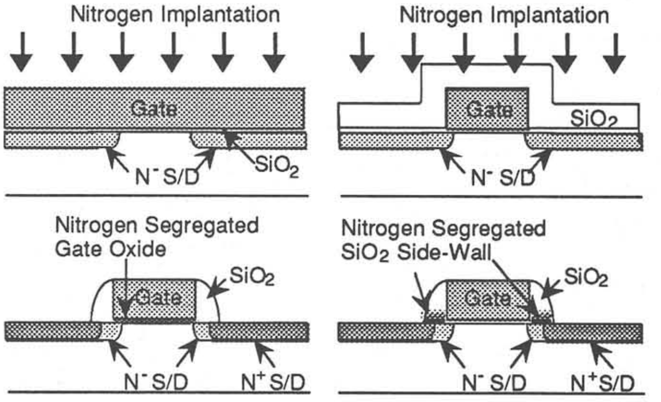
Though the supply voltage is reduced in scaling down to the sub-quarter micron region, the hot carrier degradation of MOSFETs will be continuously one of major issues. To improve hot carrier resistance, nitrided oxide has been intensively studied, employing the process of annealing the oxides in an NH_3 ambient[1)] or a N_2O ambient[2)]. Although these two nitrided oxides were known to provide an attractive hot carrier resistant structure, some disadvantages were pointed out compared with the conventional gate oxides ; lower effective mobility in the low electric field for both of the two nitrided oxides, low hot carrier resistance against the Channel Hot Electron (CHE) injection for the NH_3-nitrided oxide, and high temperature heat treatment for the N_2O-nitrided oxide. We recently proposed the novel nitrided oxide using nitrogen implantation into gate electrodes to achieve the highly reliable MOSFETs[3,4,5)]. However high nitrogen dose into gate electrodes results in the increase of the gate resistance with low temperature heat treatment used in the sub-quarter micron CMOS generation. Moreover these nitrided oxide as a gate insulator is not effective to suppress the hot carrier degradation of the LDD (Lightly Doped Drain) structure, which is mainly caused by the generation of interface state traps under the side-wall spacer[6)]. In this paper, we will present the still more reliable structure of sub-quarter micron LDD N-MOSFETs having the nitrided oxide side-wall spacer by using the simple nitrogen implantation.

2. EXPERIMENTAL

Figures 1(a) and 1(b) show the fabrication process steps of the structures with the nitrided oxide using Nitrogen Implantation into Gate Electrode (NIGE) and with the nitrided oxide side-wall spacer using the Nitrogen Implantation into the SiO_2 Side-Wall spacer (NISW), respectively. In this experiment, the gate oxide was formed in a wet ambient, and the oxide thickness was 6nm. In the NIGE structure, after the deposition of undoped amorphous silicon(200nm), nitrogen ions were implanted into polysilicon gates as shown in Fig.1(a). The gate electrodes were drawn by the electron beam direct writing. After the LDD formation using low energy ion implantation, the SiO_2 for side-wall spacers was deposited(100nm). In the NISW structure, nitrogen ions were implanted into the SiO_2 for side-wall spacers as shown in Fig.1(b). After the SiO_2 etch-back for the side-wall spacer formation, the gate electrode and the source/drain were simultaneously doped by a high dose of arsenic ion implantation. The annealing after the source/drain implantation was accomplished at less than 750°C for shallow junction formation to suppress the short channel effect.

3. RESULTS AND DISCUSSIONS

With the NIGE structure, the nitrogen implanted into the gate electrode can be incorporated in the gate oxide by heat treatment after implantation as shown in the previous reports[3-5)]. For the NIGE structure, Fig.2 shows the nitrogen depth profile in the gate polysilicon and the gate oxide film measured by SIMS. The nitrogen dose implanted into the



(a) NIGE structure with nitrided oxide by Nitrogen Implantation into Gate Electrode.

(b) NISW structure with nitrided side-wall spacer by Nitrogen Implantation into Side-Wall spacer.

Fig.1 Fabrication process steps of NIGE structure and NISW structure for highly reliable sub-quarter micron LDD N-MOSFET.

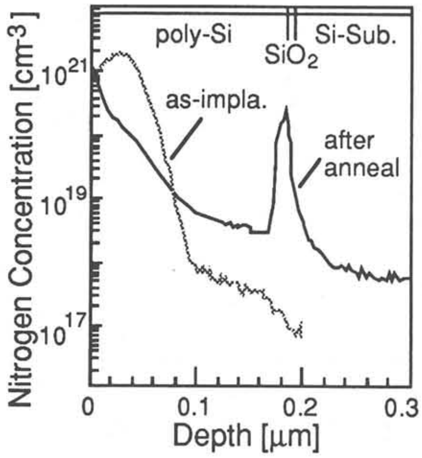


Fig.2 SIMS depth profile of nitrogen as implanted and after annealing for NIGE structure.

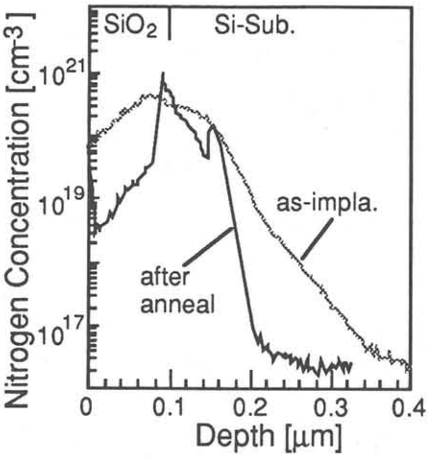


Fig.3 SIMS depth profile of nitrogen as implanted and after annealing for NISW structure.

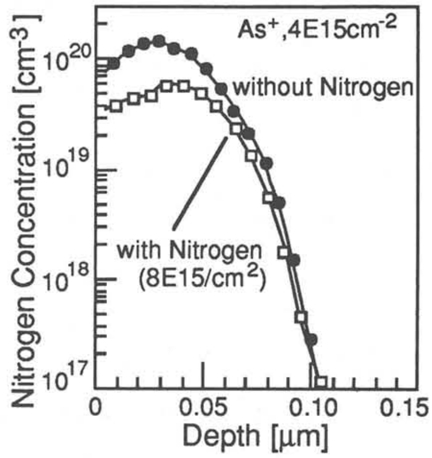


Fig.4 Comparison of activation rate of arsenic ions with and without nitrogen implantation.

gate electrodes was 4E15cm^{-2}. It can be seen that the nitrogen atoms, which are implanted into the surface region of the gate polysilicon, can easily diffuse and segregate into the gate oxide film by heat treatment after the implantation. On the contrary, for the NISW structure, Fig.3 shows the nitrogen depth profile in the side-wall SiO_2 and the Si-substrate measured by SIMS. It should be noted that the nitrogen atoms implanted into the side-wall SiO_2 can be segregated at the interface between the side-wall SiO_2 and the Si substrate by heat treatment after the implantation.

For the NIGE structure, high nitrogen dose into gate electrodes results in the increase of gate resistance and the depletion of gate electrodes with low temperature heat treatment. To analyze this increase of gate resistance and this depletion of gate electrodes, the carrier concentration depth profiles for the arsenic-implanted N^+ regions were measured by the spreading resistance technique. Figure 4 compares the carrier concentration of the arsenic ions with and without the nitrogen implantation. It should be noted that the activation rate of the arsenic ions were suppressed due to the high nitrogen dose (8E15cm^{-2}). Therefore, for the NIGE structure, as increasing the nitrogen dose, the increase of the gate resistance can be observed as shown in Fig.5. For the NISW structure, however, the gate resistance is kept the same even for the high nitrogen dose because less nitrogen atoms diffuse into the gate polysilicon. Likewise, the depletion of the gate polysilicon due to the decrease in the activation rate of arsenic can not be observed with the NISW structure.

To investigate the hot carrier hardness for the sub-quarter micron LDD N-MOSFETs, the hot carrier degradation was measured for various conditions. Figure 6 shows the comparison of the hot carrier degradation against the Drain Avalanche Hot Carrier (DAHC) injection among the conventional structure(without nitrogen implantation), the NIGE structure, and the NISW structure. It is found that the hot carrier degradation can be remarkably suppressed with the NISW structure compared with the conventional structure and with the NIGE structure. This results can be explained as follows. The hot carrier degradation of the LDD N-MOSFETs is mainly caused by the generation of

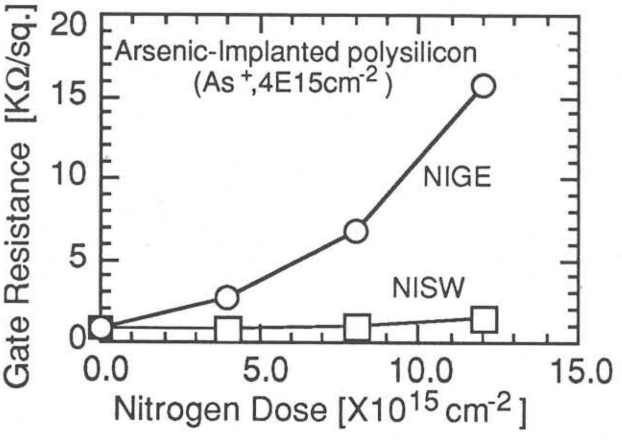


Fig.5 Nitrogen dose dependencies of gate resistance for the NIGE structure and for the NISW structure.

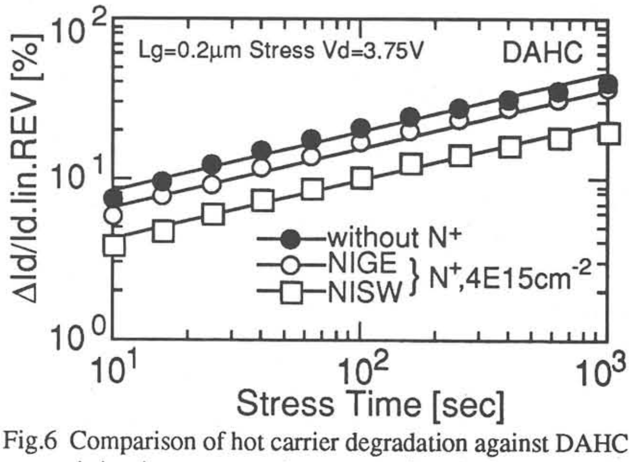


Fig.6 Comparison of hot carrier degradation against DAHC injection among the conventional structure, the NIGE structure, and the NISW structure.

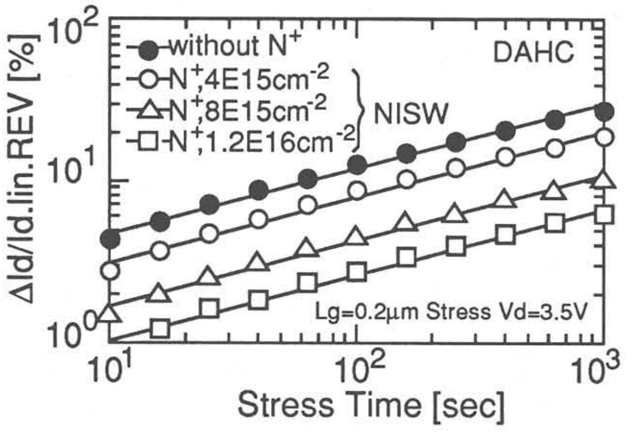


Fig.7 Nitrogen dose dependencies of hot carrier degradation against DAHC injection for the NISW structure.

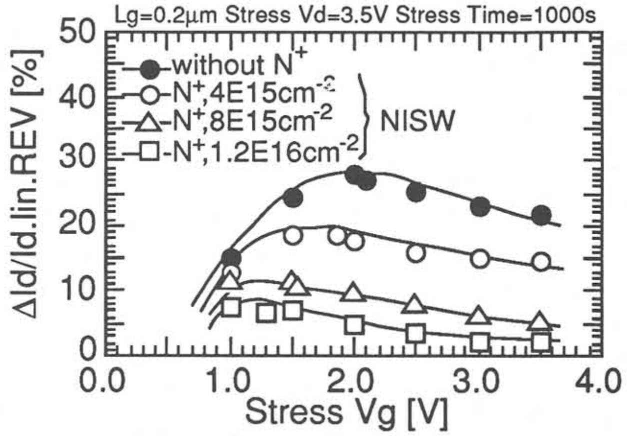


Fig.8 Dependence of hot carrier degradation on stress Vg for various nitrogen dose for the NISW structure.

the interface states in the LDD region due to the hot carrier injection into the side-wall spacer. Therefore, for the NISW structure, the nitrogen segregated between the side-wall SiO_2 and the Si substrate can reduce the generation of the interface state traps under the side-wall spacer. Figure 7 shows the nitrogen dose dependence of the hot carrier degradation against the DAHC injection for the NISW structure. It is found that the hot carrier resistance can be remarkably improved as the nitrogen dose into the SiO_2 side-wall spacer increases. From this result, the hot carrier life time for the highly nitrogen-implanted (1.2E16cm^{-2}) NISW structure is longer by two orders of the magnitude than that without the nitrogen implantation. Figure 8 shows the dependence of the hot carrier degradation on the stress Vg for various nitrogen doses with the NISW structure. It is found that, even against the CHE injection, the hot carrier resistance can be remarkably improved.

Figure 9 shows the comparison of the short channel effects for threshold voltage(Vth) and breakdown voltage of source-drain(BVds) between the NISW structure and the conventional structure. No adverse effects for the short channel effect can be observed for the nitrogen implantation into the SiO_2 side-wall spacer.

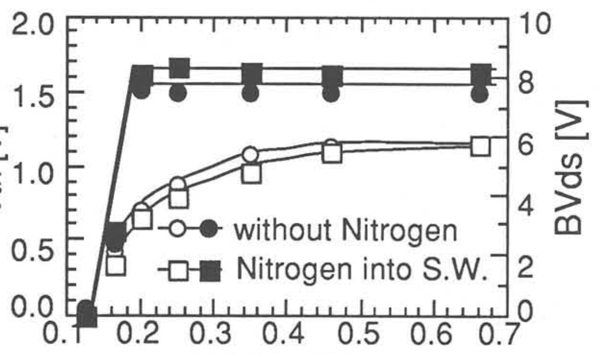


Fig.9 Comparison of short channel effect between the conventional structure and the NISW structure.

4. CONCLUSION

In conclusion, the effects of nitrogen implantation into the SiO_2 side-wall spacer for the LDD N-MOSFETs have been investigated in detail. It was found that the hot carrier degradation can be remarkably suppressed by nitrogen implantation into the SiO_2 side-wall spacer without the increase of the resistance and the depletion of the gate polysilicon caused by the decrease of the activation rate. These improvements should be due to the segregation of nitrogen atoms at the interface between the side-wall SiO_2 and the Si substrate, thus the generation of interface state traps under the side-wall spacer can be reduced. Therefore this novel structure can reduce the hot-carrier degradation of the LDD structure, which is caused by the depletion of the LDD region due to the generation of interface state traps under the side-wall spacer. Consequently, we can realize the highly reliable sub-quarter micron LDD N-MOSFETs with the simple nitrogen implantation into the SiO_2 side-wall spacer.

5. ACKNOWLEDGMENT

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