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A High Performance 0.15 μm Single Gate CMOS Technology

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High-speed 0.15 μm single gate CMOS devices have been demonstrated. We achieve the suppression of short channel effects in 0.15 μm buried channel pMOSFETs using the conventional BF_2 ion implantation process for boron counter-doping and the simple LDD structure and obtain the excellent current drive. An unloaded CMOS inverter ring-oscillator has the delay of 15.4 psec/stage when operating with a 1.5 V power supply.

1. INTRODUCTION

The trend in deep sub-micron CMOS devices has been toward dual-gate structures using n^+ poly Si gates in the case of nMOSFETs and p^+ poly Si gates for pMOSFETs.[1,2,3] These structures have become popular, because the short channel effects in p^+ poly pMOSFETs are smaller than those in n^+ poly pMOSFETs. It should be noted, however, that high-dosage boron implantations for the p^+ poly Si gate, which are required to suppress depletion layer formation at the poly-Si/gate-oxide interface, enhance boron penetration through the gate oxide into the channel region to significant levels. Hence, a single gate structure using n^+ poly Si gate for both nMOSFETs and pMOSFETs is attractive even in sub-micron CMOS devices. Further, buried channel (BC) pMOSFETs are superior to surface channel (SC) pMOSFETs, since hole mobilities in BC pMOSFETs are much greater than in SC pMOSFETs. However, the application of BC pMOSFETs to deep sub-micron CMOS devices requires a shallow counter-doped region to suppress the significant short channel effects. To realize a 0.15 μm BC pMOSFET for 2 V operation, we have previously proposed a solid phase diffused channel (SPDC) pMOSFET.[4] On the other hand, Fig. 1 shows that short

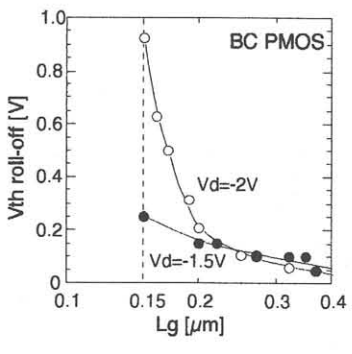

Fig.1 Vth roll-off vs. gate length

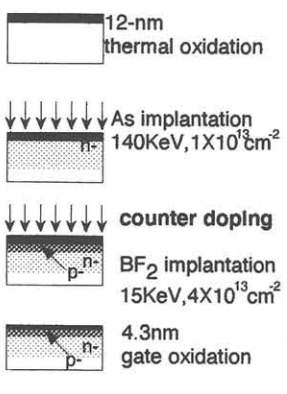

Fig. 2 Process of buried channel formation

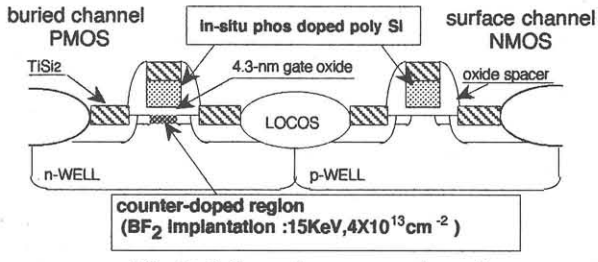

Fig. 3 Schematic cross section of the single-gate CMOS

channel immunity could be achieved in a 0.15 μm BC pMOSFET for 1.5 V operation, even with the usual BF_2 ion implantation process. The procedure for counter-doping is described in Fig. 2. This paper describes a high performance 0.15 μm single gate CMOS device using the simple BF_2 implantation process for boron counter-doping for the first time.

2. EXPERIMENTAL RESULTS

A schematic cross section of the single-gate CMOS

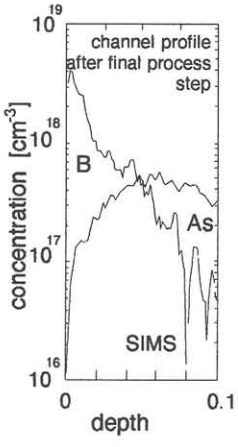

Fig. 4 SIMS profiles

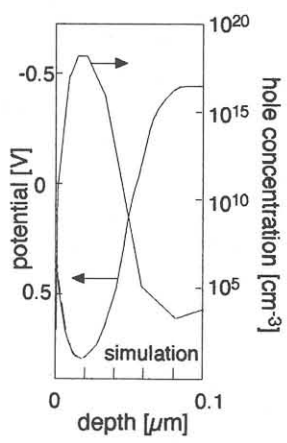

Fig. 5 Simulation results

device is shown in Fig. 3. An in-situ phosphorus-doped poly Si gate and Conventional LDD structures are used for both n-MOSFETs and pMOSFETs. The gate oxide thickness is 4.3 nm. Self-aligned Ti silicide is used to reduce

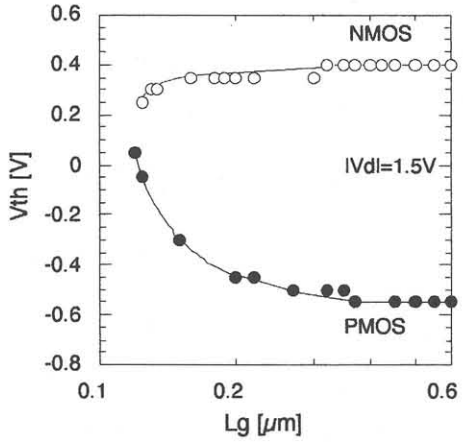

Fig. 6 Vth vs. gate length

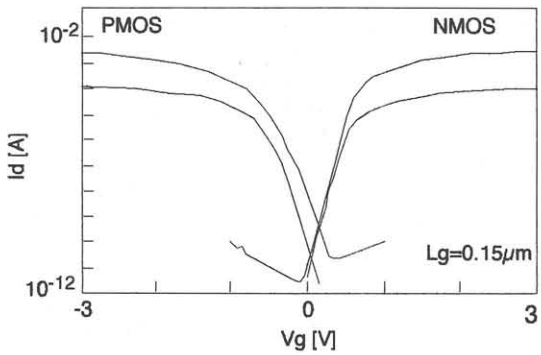

Fig. 7 Subthreshold characteristics of 0.15μm MOSFETs (|Vd|=50mV, 1.5V)

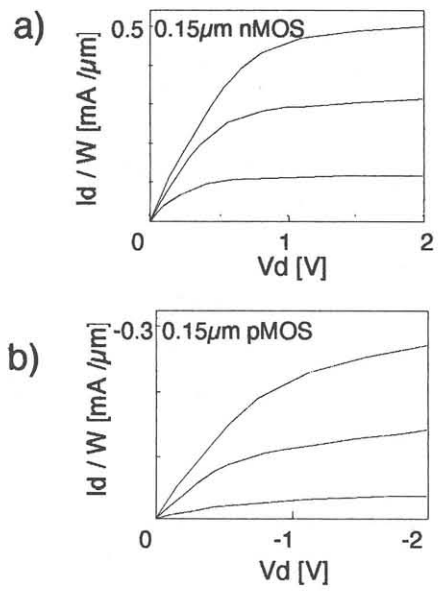

Fig. 8 Id vs. Vd (Vg steps from 0V to 2V.) (a) nMOSFET (b) pMOSFET

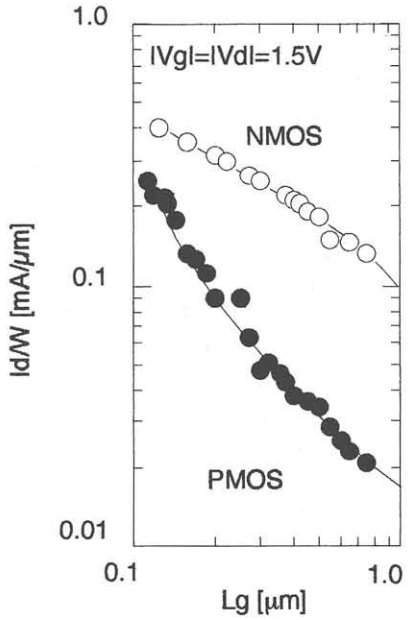

Fig. 9 Drain current vs. gate length

parasitic resistances with a 0.1 μm oxide spacer. The channel profile of the BC pMOSFETs is shown in Fig. 4. Counter-doping is carried out using the conventional BF_2 ion implantation process. The junction depth and surface concentration of this region are 50 nm and 4 x 10^{18} cm^{-3}, respectively. Figure 5 shows the result of a two-dimensional device simulation for potential and carrier profile in this channel. The depth of the buried channel is as shallow as 0.02 μm from the surface. The gate length dependence of threshold voltage is shown in Fig. 6. At a gate length of 0.15 μm, Vth roll-off in pMOS and nMOS devices are 0.25 V and 0.1 V, respectively. Figure 7 shows the subthreshold behaviors for 0.15 μm pMOS and nMOS devices. These devices operate well without punch-through, even at 1.5 V. The Id-Vd characteristics are shown in Fig. 8. The channel length dependence of drain current and saturated

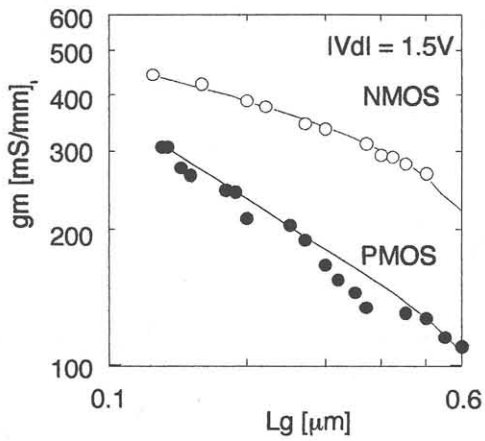

Fig. 10 Saturated transconductance vs. gate length

transconductance (gm) in 1.5 V operation are shown in Figs. 9 and 10, respectively. Consequently, the use of BC pMOSFETs in 0.15 μm CMOS devices achieves excellent

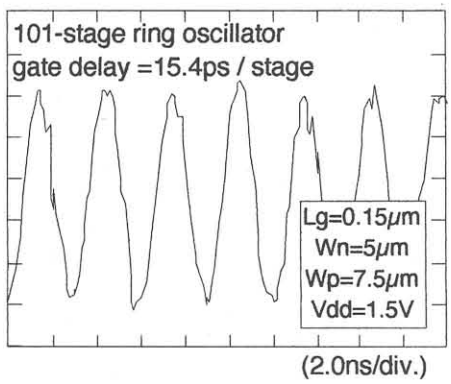

Fig. 11 101-stage ring oscillator output waveform

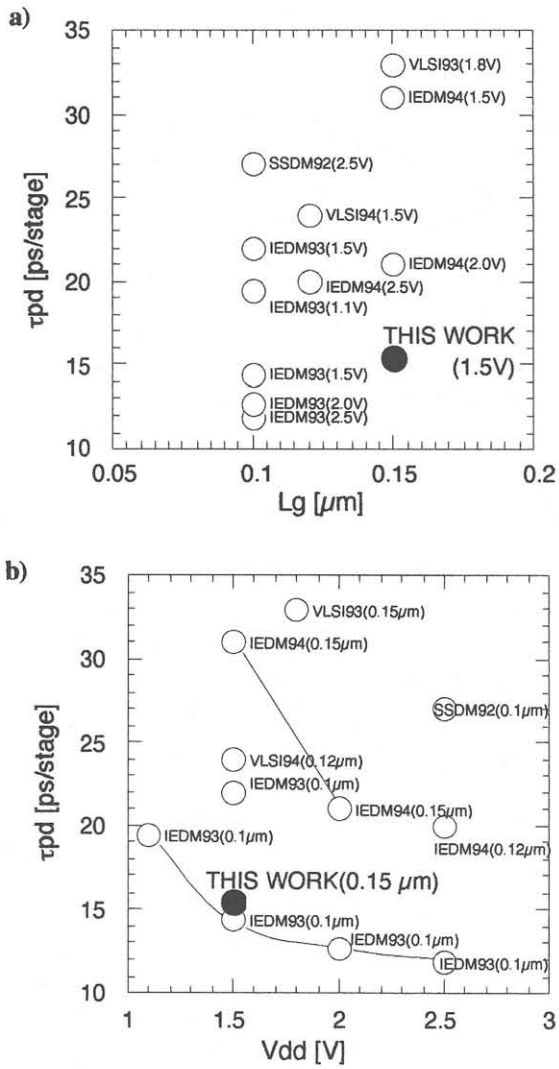

Fig. 12 Gate delay comparisons at room temperature
a) gate length dependence
b) operation voltage dependence

Device parameters and performances	NMOS	PMOS
Lg [μm]	0.15	
threshold voltage [V]	0.35	-0.30
Vth roll-off (IVdl=1.5V) [V]	-0.10	0.25
subthreshold swing (IVdl=1.5V) [mV/decade]	81	99
saturated gm (IVdl=1.5V) [mS/mm]	422	264
Id (IVdl=IVgl=1.5V) [mA/μm]	0.36	0.18
Gate Delay (F/O = 1, Vdd =1.5V) [ps/stage]	15.4	
power [μW/stage]	165	

Table. I 0.15μm single gate CMOS device parameters and performances

current drive. However, the falling gradient of the curve showing the dependence of saturated gm on gate length reflects the effect of parasitic resistances in the source and drain regions of both sub 0.2 μm nMOS and pMOS devices. Figure 11 shows the output waveform of a 0.15 μm unloaded CMOS inverter ring oscillator with 101 stages operating at 1.5 V. The propagation delay per stage is 15.4 psec at 1.5 V. This delay time is the smallest value reported for any 0.15 μm CMOS device. Moreover, it is similar to the minimum delay reported for 0.1 μm CMOS devices at the same operating voltage, as shown in Fig. 12. The device parameters and measured results for 0.15 μm single gate CMOS devices are summarized in Table I.

3. CONCLUSION

High-performance 0.15 μm single gate CMOS devices for 1.5 V operation have been demonstrated. The conventional BF_2 ion implantation process for boron counter-doping achieves suppression of short channel effects and excellent current drive, even using the conventional LDD structure for simple fabrication. An unloaded CMOS inverter ring-oscillator was shown to have the delay of 15.4 psec/stage when operating with a 1.5 V power supply.

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