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Characteristics of Conductivity Modulated Polysilicon Thin Film Transistors

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This paper reports the characteristics of a novel high voltage Conductivity Modulated Thin Film Transistor(CMTFT) fabricated using polycrystalline silicon. The transistor uses the idea of conductivity modulation in the offset region. Experimental results show that the CMTFT has significantly higher on-state current handling capability compared to that of the conventional offset drain device while still maintaining low leakage current and providing even faster switching speed. The CMTFT devices can be fabricated using a low temperature process (600°C) which is highly desirable for large area electronic applications.

1. INTRODUCTION

Polycrystalline silicon thin film transistors (TFTs) fabricated at low temperature have attracted much attention in various large area electronic applications such as flat panel displays, page width optical scanners and page width printer heads. In conventional TFT, the drain has to be offsetted from the channel region in order to achieve low leakage current. However, this causes severe current pinching problem, resulting in high on-resistance. The problem is even more severe in high voltage TFT devices since a longer offset region is needed for providing the high voltage. To alleviate the current pinching problem, a low concentration implant was used to dope the offset region[1]. However, the required implant charge density is extremely difficult to determine. Recently a field plated high voltage TFT was proposed to solve the problem[2]. It offers higher current driving capability while still maintaining low leakage. However, this approach results in a complicated device structure and biasing scheme[3]. This paper reports a novel high voltage Conductivity Modulated Thin Film Transistor (CMTFT) fabricated using polycrystalline silicon. The transistor uses the idea of conductivity modulation in the offset region to obtain a significant reduction in on-state resistance. With this structure, the offset implant and the complicated field plate scheme used in the offset drain TFT can be avoided.

2. DEVICE STRUCTURE & OPERATION

The schematic cross-section of the offset drain TFT and CMTFT are shown in Fig. 1(a) and (b) respectively. The offset drain TFT is a majority carrier device and has an offset region placed between the drain and channel region for low leakage current and high breakdown voltage. In the CMTFT structure, conductivity modulation in the offset drain region is implemented by incorporating a p^+ drain region instead of an n^+ drain region conventionally used in the offset drain TFT. At a gate voltage above the threshold voltage and a high enough drain to source voltage, holes are injected from the p^+ drain into the offset region and the electrons are flowing in from the channel. The injected holes recombine with the grain boundary traps and facilitate the flow of electrons in the offset region. The high concentration of injected holes in the offset region conductivity modulate the region and provide much lower on-resistance compared to that of the conventional offset drain TFT. To contact the channel region of the device, a segmented source structure as shown in Fig. 1(b) is used.

3. EXPERIMENTAL RESULTS & DISCUSSION

Both n-channel CMTFT and offset drain TFT were fabricated using a low temperature process (600°C) on the same substrate. A 1200 °A active poly-Si film was prepared by solid phase crystallization method. A 1000 °A APCVD gate oxide was used. In the case of the conventional offset drain TFT, an implant dose of $1x10^{12}$ cm^{-2} was used to dope the offset region. The devices were hydrogenated by depositing a

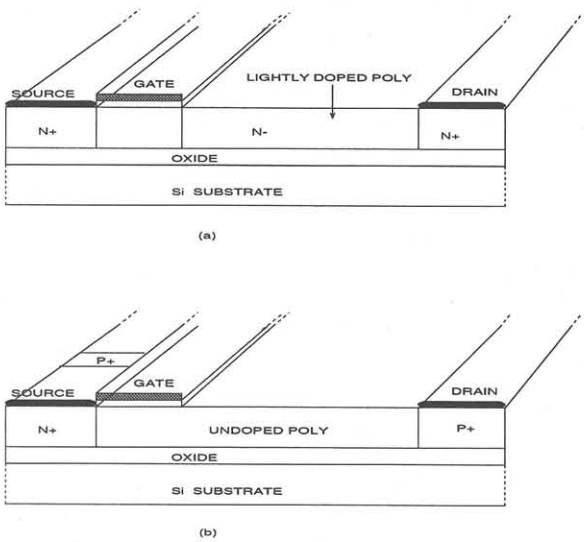

Fig. 1: Schematic cross-section of (a)Conventional offset drain TFT and (b) CMTFT.

PECVD silicon nitride cap layer at 300°C with a thickness of 3500 °A and annealing in forming gas at 400°C for 90 minutes.

Fig. 2 compares the forward conduction characteristics of the offset drain TFT with that of the CMTFT. Both devices are with identical dimensions and have an offset length (L_{OFF}) of 3μm and W/L ratio of 50/5. The offset drain TFT suffers from severe current pinching effect due to the existence of the high resistive lightly doped polysilicon offset region. In the case of the CMTFT, at a gate voltage above the threshold voltage and drain voltages below 0.7V, the p^+ drain is off and no holes are injected from the p^+ drain into the offset region. The device is basically off and the trapped charge density at the grain boundaries are not changed. Thus, the resistivity of the offset region remains high. When the drain voltage is larger than 0.7V, the p^+ /offset region junction at the drain is turned on. At higher drain voltages, the amount of hole injection increases and a significant interaction between the injected holes and the grain boundary traps occurs. Depending upon the energy of the traps, the holes may recombine with trapped electrons, or themselves be trapped. In either case, lowering of the barrier height formed between grain boundaries results. This reduction in barrier height facilitates the flow of both electrons and holes. Due to the increase in both electron and hole concentration in the offset region, the resistance of the offset region is modulated and reduced drastically. This in turn increases the current handling capability of the device. As the drain voltage is further increased, channel pinching occurs, and the CMTFT experiences drain current saturation which is similar to that occurs in conventional MOSFET. From Fig. 2, at a gate voltage of 20V and drain voltages ranging from 5V to 20V, the on-state current of the CMTFT is three orders of magnitude to one order of magnitude higher than that of the offset drain TFT.

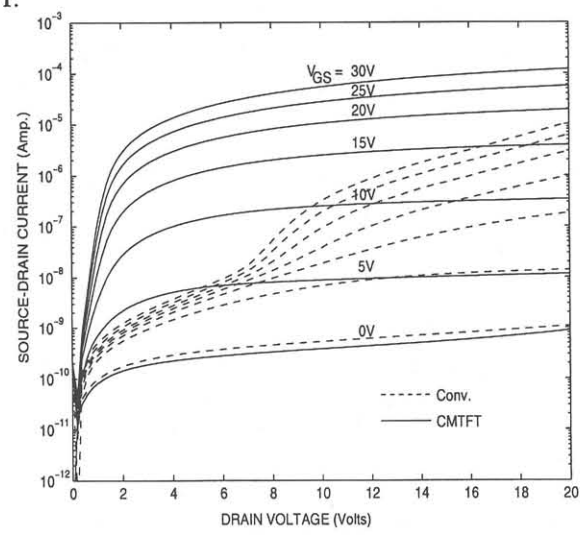

Fig. 2: Forward conduction characteristics for the conventional offset drain TFT and CMTFT with L_{OFF}=3μm and W/L=50/5.

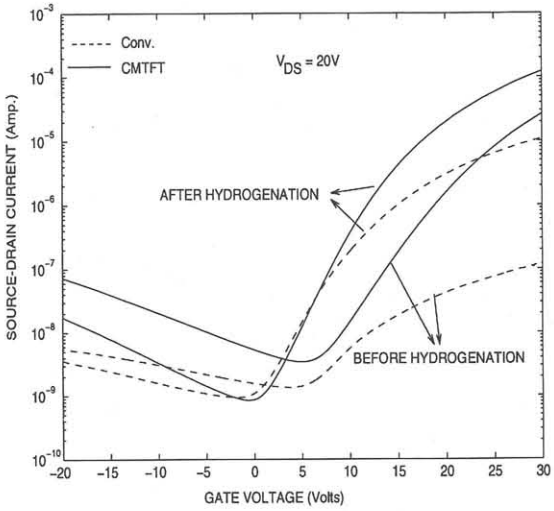

Fig. 3: I_{DS}-V_{GS} curves at V_{DS}=20V for devices with L_{OFF}=3μm and W/L=50/5 before and after hydrogenation.

The gate transfer characteristics for both structures before and after hydrogenation are compared in Fig. 3. The dependence of leakage current on the gate and drain voltage for both the devices is similar before and after hydrogenation. The threshold voltage, subthreshold slope and leakage current are all reduced for both of the structures after hydrogenation. Fig. 4 shows the leakage current characteristics of both the structures when the offset length is changed. The amount of leakage current measured for the CMTFT is less than that of the conventional TFT and comparable to that reported in the literature[1].

Fig. 5 shows the temperature dependence of the leakage current for both structures. Both of them experience higher leakage current as the temperature increases. At low V_{DS}, the activation energy for source-drain current conduction is around 0.54eV for both structures. However, as V_{DS} is increased, the activation energy of the offset drain TFT is reduced because of the Pool-Frenkel effect. But in the case of the CMTFT, the activation energy is increased at higher V_{DS} which implies that the source-drain current conduction is not limited by the Pool-Frenkel effect. At low V_{DS} , the CMTFT shows a 40 percent reduction in leakage current compared to that of the offset drain TFT for the temperature range from 10°C to 120°C. At a V_{DS} of 20V and temperature close to 120°C, both structures experience similar leakage current characteristics.

Since the CMTFT involves minority carriers for conductivity modulation, the switching speed of the device might be affected by the minority carrier storage effect. However, the minority carrier lifetime measured from the reverse characteristics of diodes formed within a polysilicon sample with sub-micron grain size is of the order of 20-100ps[4]. Therefore, the transient behavior of the CMTFT is not expected to

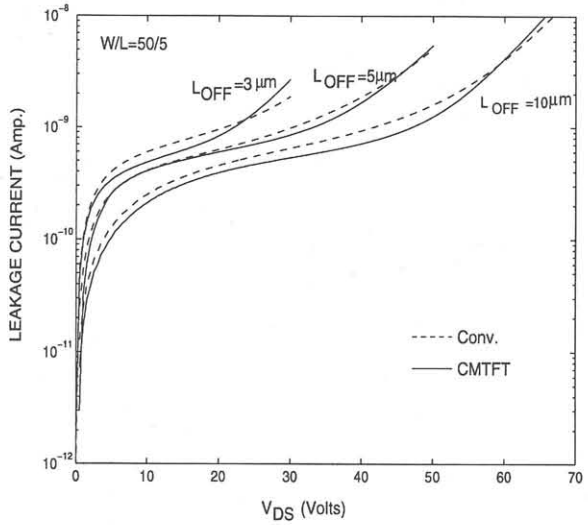

Fig. 4: Leakage current characteristics with various offset lengths.

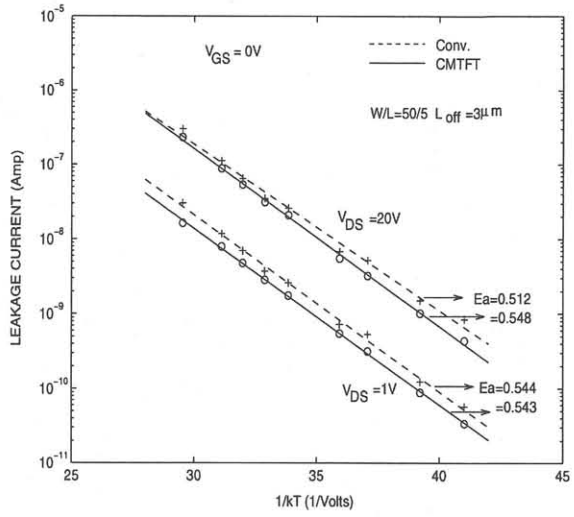

Fig. 5: Leakage current versus 1/kT for the conventional offset drain TFT and the CMTFT at low and high V_{DS}.

be degraded compared to the conventional one. The transient characteristics of the offset drain TFT and CMTFT were measured by using a resistive load connected between the drain and power supply with the source grounded. Fig. 6 shows the switching waveforms. To compare the switching performance, both devices were biased at the same drain to source and gate to source voltage of 18V and 20V, respectively. The identical drain to source voltage for both devices was obtained by adjusting the value of the load resistance. As expected, the turn-off time of the CMTFT (43.2μs) is not degraded compared to that of the conventional offset drain TFT (162.8μs), and in fact a factor of 3.8 times improvement is observed in the CMTFT due to the higher current sourcing capability. The turn-on time of the CMTFT and conventional TFT is 21μs and 67.4μs, respectively. The 3.2 times reduction in turn-on time in the CMTFT is due to the much smaller on-resistance which discharges the parasitic capacitance of the system faster.

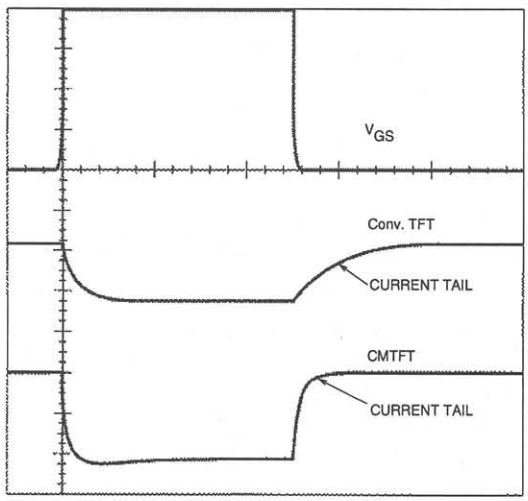

Fig. 6: Switching waveforms for the conventional offset drain TFT and CMTFT. Trace: 5V/div and Time scale: 200μs/div.

4. CONCLUSION

The characteristics of a new device structure called the Conductivity Modulated Thin Film Transistor (CMTFT) is reported. Using this structure the current pinching problem in low leakage offset drain TFT devices can be eliminated. It is shown that the CMTFT has higher current handling capability than that of the conventional offset drain TFT while still maintaining low leakage current and providing even faster switching speed.

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