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Simulation of Enhanced Drain Current Characteristics in a MOSFET with a Quantum Wire Structure Incorporating a Periodically Bent Si-SiO_2 Interface

Junko TANAKA and Akemi SAWADA

Central Research Laboratory, Hitachi, Ltd.
1-280 Higashi-koigakubo, Kokubunji, Tokyo 185, Japan

A quantum wire structure with a periodically bent S-SiO_2 interface has been studied through simulations. Electron confinement effect by a bent Si-SiO_2 interface is clearly observed at low gate voltage and is reduced as the gate voltage becomes higher. A MOSFET with this quantum wire structure shows excellent subthreshold characteristics and enhanced drive capability compared to a conventional MOSFET with a flat Si-SiO_2 interface.

1. INTRODUCTION

It has been theoretically predicted that ultrafine semiconductor quantum wire structures will bring about an increase in electron mobility due to lateral electron confinement and can be used in high speed devices.[1] Recent study using simulations has shown that a quantum wire structure with a periodically bent interface of *n*-AlGaAs/*u*-GaAs heterojunctions can contain one-dimensional electron-gas systems, where electrons are more accumulated in convex regions of the *u*-GaAs layers than that in the concave ones.[2, 3]

Recently, several silicon quantum wire structures have been proposed and their excellent electron confinement has been demonstrated.[4-6] Quantum wire structures fabricated using silicon material are promising in the post-ULSI era rather than that using compound materials, because of their high productivity and reliability. However, most studies on quantum wires have been made to investigate quantum phenomena; thus the effects of applying these structures to actual devices have not been addressed.

In this paper, we report on a quantum wire structure with a periodically bent Si-SiO_2 interface by simulations, and show the superior simulated performance of a MOSFET with this quantum wire structure compared to that of a conventional MOSFET with a flat Si-SiO_2 interface.

2. DEVICE STRUCTURE AND SIMULATION METHOD

A schematic cross-sectional view of the simulated MOSFET is shown in Fig. 1. The Si-SiO_2 interface is bent with a period of 0.1 μm and a bending angle of 90°. The effective geometrical width W_{eff} along the Si-SiO_2 interface is $\sqrt{2}$ W, where W is the width in the *x* direction.

In the analysis, a nonplanar device simulator [7-9] was used, in which an arbitrary trapezoidal grid was used to discretize the simulation domain with a nonplanar interface.

3. RESULTS AND DISCUSSION

In order to examine the electron confinement effect by a periodically bent Si-SiO_2 interface, the potential and electron density distributions were calculated at the center of the channel. Calculated surface potential distributions along the Si-SiO_2 interface are shown in Fig. 2. The results for the structure with a flat Si-SiO_2 interface are also shown for comparison. Because electric fields concentrate in the convex region, the potential in the convex region is higher than that of the flat structure for each gate bias voltage. The potential at point A in the convex region is 0.32 V higher than that at point B in the concave region at a gate voltage of 0.0 V. This increase

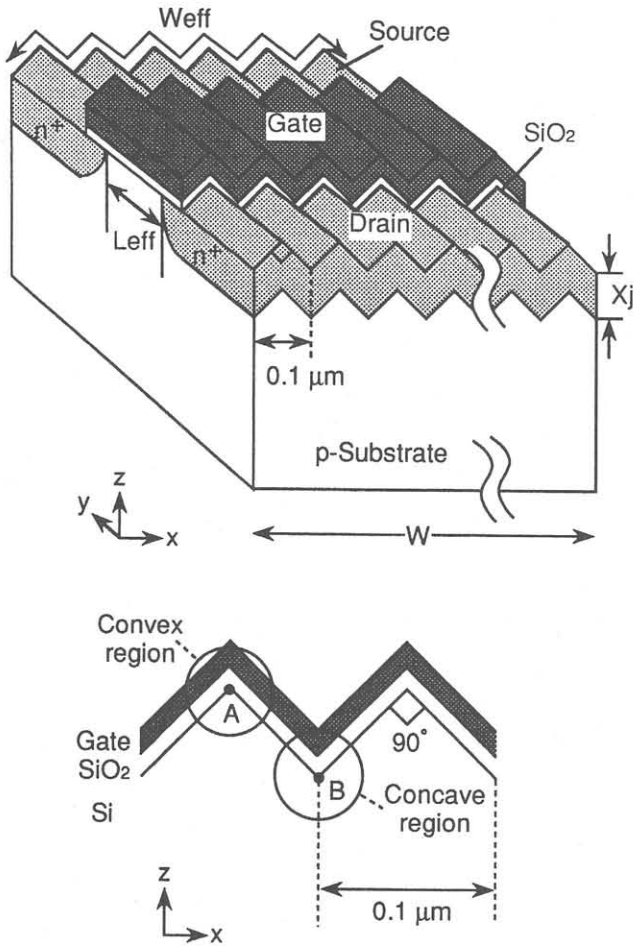

Fig. 1. A schematic cross-sectional view of the simulated MOSFET with a bent Si-SiO_2 interface. Device parameters are Leff = 0.3 μm, Nsub = 3.0 x $10^{17}cm^{-3}$, Xj = 0.1 μm, and W = 10 μm.

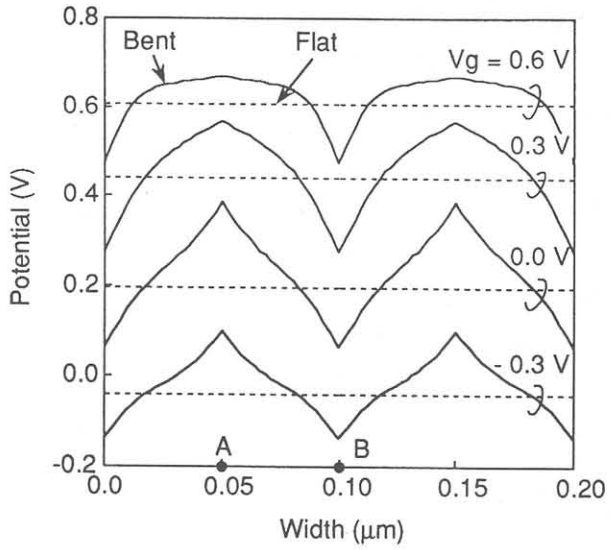

Fig. 2. Calculated surface potential distributions along the Si-SiO_2 interfaces of the bent and flat structures for different gate voltages. Vs = 0 V and Vd = 1.5 V.

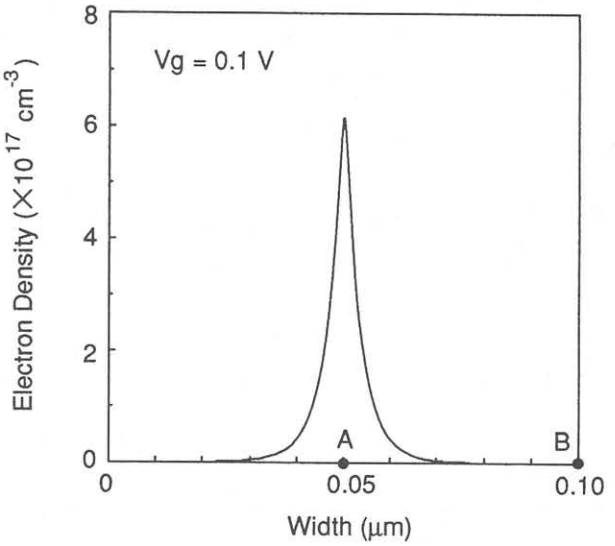

Fig. 3. Calculated electron density distribution along the Si-SiO_2 interface of the bent structure. Vs = 0 V and Vd = 1.5 V.

in potential in the convex region enables us to obtain fine electron confinement in the convex region. As a result, as shown in Fig. 3, a narrow channel is created with a width in the order of 10 nm, which is much narrower than the bending period of 0.1 μm. As the gate bias voltage increases, the difference in potential between points A and B becomes smaller and thus the electron confinement effect is reduced.

The drain current characteristics of the bent and flat structures are compared in Fig. 4. Higher drain current flows in the bent structure than in the flat structure (Fig. 4(a)), because a higher potential is obtained in the convex region of the bent structure than in the flat structure at the same gate voltage. The subthreshold swing of the bent structure is observed to be 64 mV/decade, and that of the flat structure is 74 mV/decade. The subthreshold swing of the bent structure is 14% smaller than that of the flat structure due to the rapid increase in potential in the convex region that accompanies an increase in the gate bias voltage at low levels (Fig. 2). Figure 4(b) shows drain current characteristics of the bent structure against those of the flat structure. It is clearly seen that the bent structure shows enhanced drain current characteristics,

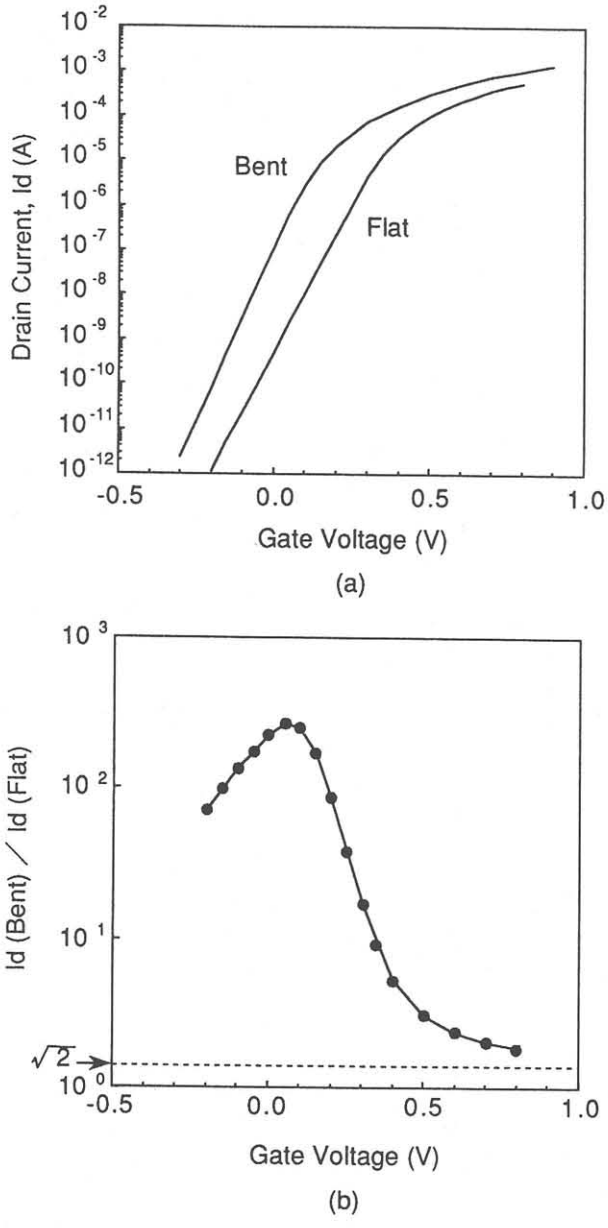

Fig. 4. Calculated drain current characteristics of the bent and flat structures: (a) Subthreshold characteristics, (b) Drain current characteristics of the bent structure against those of the flat structure. Vs = 0 V and Vd = 1.5 V.

indicating a maximum at around V_g = 0.05 V, where the drain current is 270 times higher than that of a flat structure. Due to electron confinement effect, the drain current of the bent structure is more than $\sqrt{2}$ (= W_{eff} / W) times higher than that of the flat structure for all gate voltages simulated. As the gate bias voltage becomes much higher, the ratio of the drain current of the bent structure to that of the flat structure approaches $\sqrt{2}$.

4. CONCLUSIONS

We have investigated a quantum wire structure with a periodically bent Si-SiO_2 interface through simulations, and have shown that this structure provides excellent subthreshold characteristics and enhanced drive capability compared to a conventional MOSFET with a flat Si-SiO_2 interface.

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