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Analysis of Chaos in Capacitance-npn-Transistor Pair and Its Application to Neuron Element

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Chaotic response of capacitance-npn-transistor pair was proved at first via qualitative analysis, experiment and simulation. This circuit is very simple compared with chaos-generating circuits that have been proposed and can be implemented by typical BiCMOS process, yet its characteristics contains many functions and is easily controllable. We simulated characteristics of the neuron circuit using this circuit in detail. The simulated results shows the feasibility to realize a novel information processing system such as chaotic neural networks.

1 Introduction

We experimentally found chaos in thyristors[1] and have clarified its physical mechanism utilizing a coupled pnp-npn transistor model[2,3], aiming to realize a novel, multi-functional device/circuit for information processing. Through this study, we found that role of the pnp transistor in the model is simply as a capacitance. Here, we report the characteristics of chaos in a simplified circuit that is consisted of a capacitance and an npn transistor. Then we propose a novel neuron circuit using this circuit, which can be realized by typical BiCMOS techniques. This circuit has various remarkable characteristics and is much simpler than the circuits that have been proposed to realize neural networks in hardware[4].

2 Circuit and Mechanism

Figure 1(a) shows the fundamental circuit of a capacitance-npn-transistor system. A capacitance is connected to the collector of an npn transistor and an ac voltage is applied between the further end of the capacitance and the emitter. A constant current is fed to the base of the transistor. Replacing the transistor by its equivalent circuit that contains parasitic capacitances, we obtain Fig. 1(b), in which the symbols are introduced. During a positive half cycle of the ac voltage, I_b charges C_e and v_{be} rises gradually. When v_{be} exceeds the threshold voltage V_{th}, the forward collector current i_F with the amount of $\beta_F \cdot I_b$ flows and charges the external capacitor

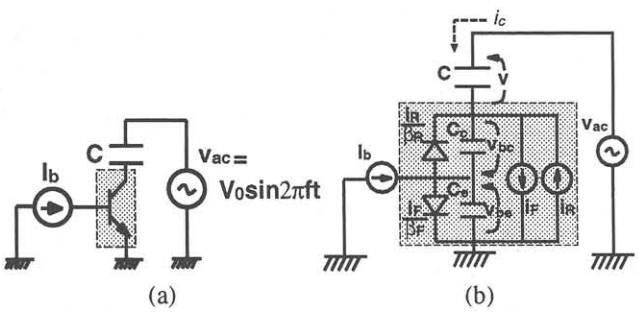

Fig. 1. (a) Fundamental circuit of capacitance-npn-transistor circuit. (b) Equivalent circuit which includes parasitic capacitance in the npn transistor.

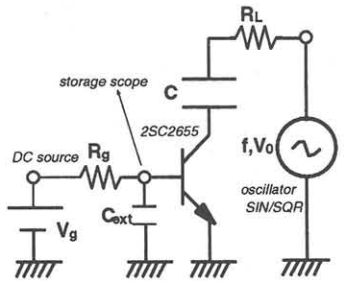

Fig. 2. Experimental circuit. NPN transistor is type 2SC2655, $C = 4.7$nF, $R_g = 1\text{M}\Omega$, $R_l = 1\text{k}\Omega$ and $C_{ext} = 680$pF

C. If v_{be} does not reach V_{th}, the collector current does not flow. During the negative half cycle, reverse current flows to discharge C, and in this process v_{be} drops by the reverse displacement current that is large when the reverse current is large. At low frequency, the system repeats charging and discharging in every half cycle as described above. However, when the oscillation frequency f is within a proper region near the charging time of C_e determined by I_b and C_e, the charging and discharging become incomplete and leave the effect in the succeeding half cycle. Mathematically, this means the first-return-mapping and results in period doubling and chaos as in the case[2,3] of thyristors. We show the aspects of chaos clarified by experimental results and SPICE circuit simulator in the following sections.

3 Experimental Results

In the previous section, it is described qualitatively that a capacitance-npn-transistor circuit shows chaotic response within the proper parameter region. This can be confirmed experimentally with the pair of a discrete npn-transistor and a capacitor as shown in Fig.2.

A dc voltage source(V_g) and a resistance R_g are used for a current source, and an additional resistance (R_L) is connected between C and ac voltage source. These changes are not essential for the generation of chaos. An additional capacitor C_{ext} is connected in parallel with the base-emitter junction to satisfy $C_c \leq C_e + C_{ext}$ and to eliminate the displacement current while $dv_{ac}/dt > 0$, where C_c and C_e

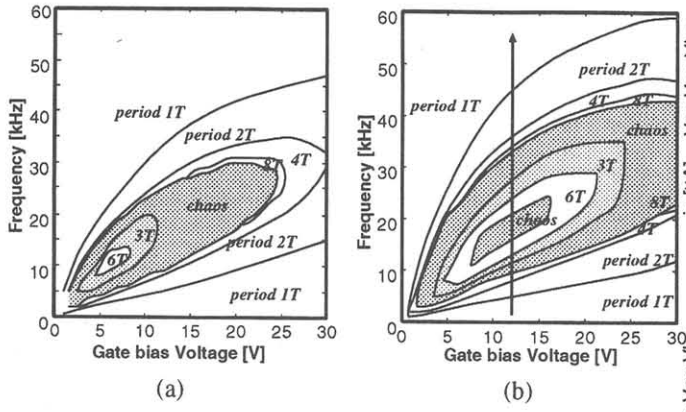

Fig. 3. Measured parameter region (V_g, f) in which the system result in period-multiplying / chaotic states, (a) under sinusoidal- and (b) square-wave excitation.

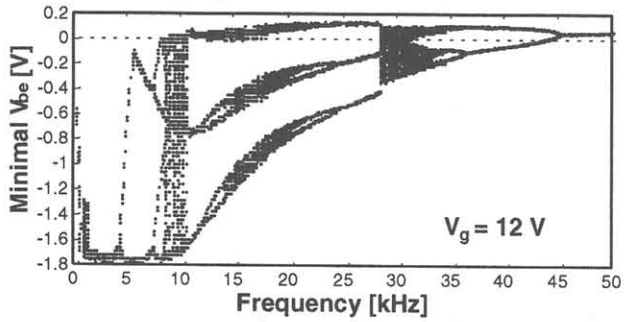

Fig. 4. Measured bifurcation diagram

are the collector- and emitter stray capacitances. Then the chaotic response is observed within wider parameter region than the case without C_{ext}.

The circuit parameters used in the experiment are C = 4.7nF, R_L = 1kΩ,R_g = 1MΩ and C_{ext} = 680pF, and device parameters of the transistor have been estimated from the measurement as C_e = 340pF, C_c = 64pF (when zero biased), β_F = 140 and β_R = 14. The amplitude of the oscillator is set at V_0 = 5V.

Figure 3 indicates the parameter region of (V_g, f) within which the v_{be} shows periodic or chaotic response under (a) sinusoidal- and (b) square-wave excitation, respectively. Though each result shows the similar bifurcating route to chaos, the parameter region is wider in the case of square-wave excitation than the case with sinusoidal excitation. Figure 4 shows the bifurcation diagram of the minimal voltage of v_{be} by changing f with V_g fixed at 12V in the case of square-wave excitation.

4 Simulation Results

The qualitative discussion described in §1 would applied

Table 1. Assumed device parameters of an npn-transistor (in the form of spice3e2 BJT model)

CE	10fF	MJE	0.33	BF 100	BR 1
CC	3fF	MJC	0.5	TF 0.35ps	TR 0.35ns
CS	30fF	MJS	0.5		C 50fF

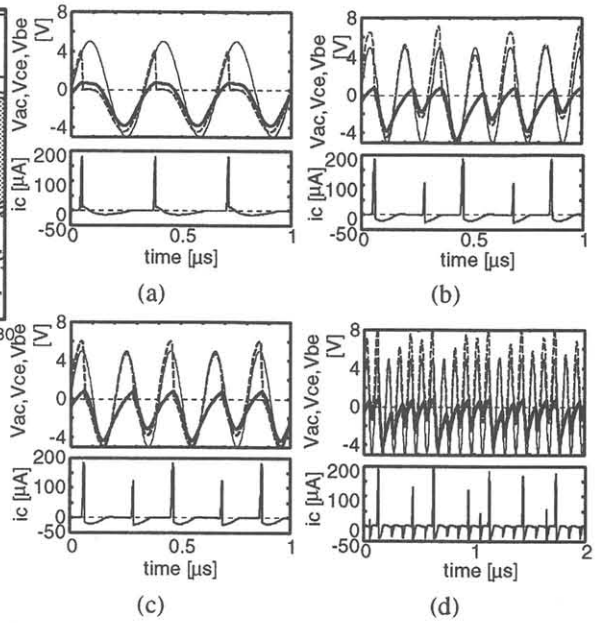

Fig. 5. Simulated waveforms of v_{ac}, v_{ce}, v_{be} and i_c. (a) f = 3 MHz (period 1) (b) 4.8 MHz (period 2) (c) 5.6 MHz (period 4) (d) 10 MHz (chaos).

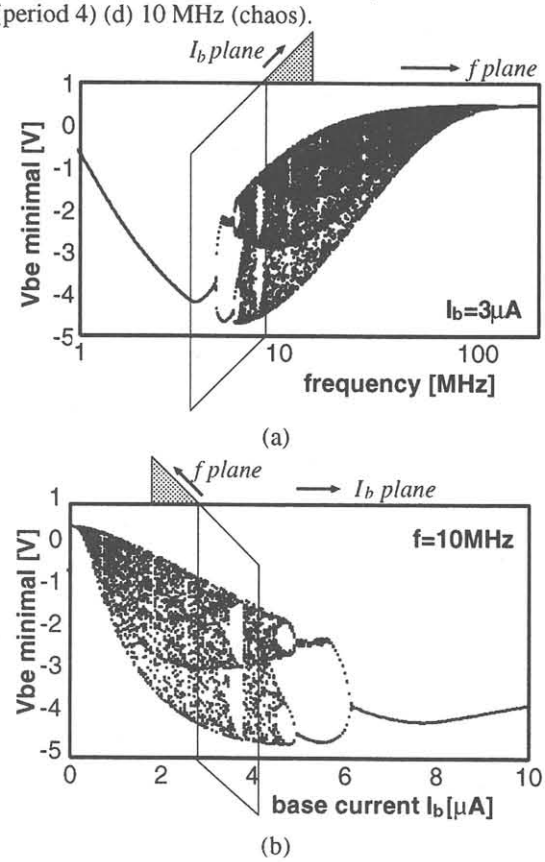

Fig. 6. Simulated bifurcation diagram of minimal v_{be} according to (a) f with I_b = 3μA and (b) I_b with f = 10MHz.

to the circuit fabricated by recent technology, assuming each parameter to be scaled properly, with the frequency region for the chaotic response becoming higher. To confirm this, we simulated the characteristic of the system which is assumed to be fabricated by recent BiCMOS process technology with

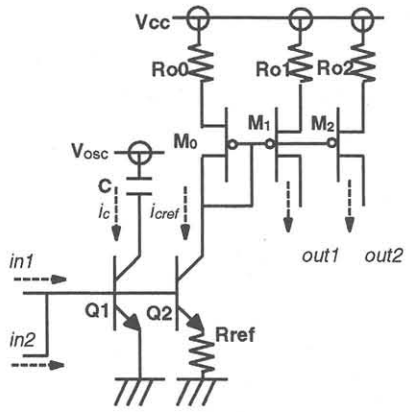

Fig. 7. Proposed application of capacitance-npn-transistor circuit to a neuron element.

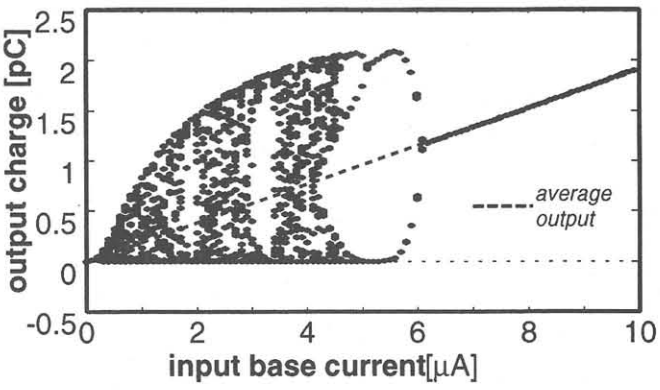

Fig. 8. Net charge of i_{cref} in a positive half cycle according to input current. Dashed line in the schematic expresses the average of the output charge.

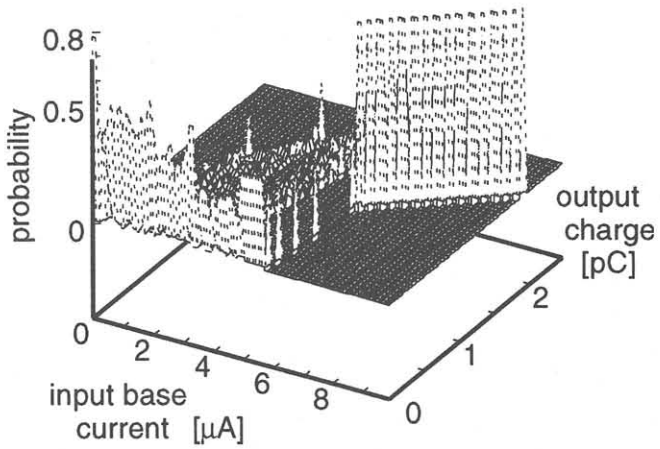

Fig. 9. Histogram of output charge according to input current.

its device parameters shown in Table1.

Figures 5(a)-(d) show the simulated waveforms of the voltages v_{ac}, v_{ce}, v_{be} and the amount of supplied current from the ac source (i_c). Figures 5(a) shows the period 1 state at a low enough frequency. Increasing the frequency, period 2 and period 4 states appear (Figs. 5(b) and (c)) , and chaotic state (Fig. 5(d)) is finally seen. In this state, the variations of the voltage and the load current seems to be random. The route to chaos can be best visualized in the change of the minimal voltage of v_{be} as shown in the bifurcation diagram of Figs. 6(a) and (b). Figure 6(a) shows the change in the minimal voltages according to the change of the parameter f. Figure 6(b) shows those with the change in I_b. Each diagram shows period-doubling-type chaotic sequence.

5 Hardware implementation and its Application

Figure 7 shows one proposal of the application of this circuit as an element of a neural network. Determined by input current I_b (assumed constant in this study), the pair of C and Q_1 which are ac-driven by V_{OSC} shows periodic or chaotic response as described in § 4. The base of Q_2 is biased at the same voltage as the base voltage of Q_1, so the collector current of Q_2 that is proportioned to the collector current of Q_1 flows and this current becomes outputs to outer element via the current mirror circuit of M_0, M_1, M_2, $\cdots$, weighed by the resistance R_{o1}, R_{o2}, $\cdots$. The output pulsed-current is statistically larger as the input current is larger. If f is set within a proper region, the amount of output charge varies at every cycle, as seen in Fig. 8, and the value is unpredictable even mathematically.

Figure 9 shows the histogram of the amount of output charge against input current at the same condition as in Fig. 8. In the chaotic region, the probability distribution is widely distributed although the probability of taking a lower value is relatively larger. On the contrary, it has sharp edges in the periodic region. The states are easily controlled as deterministic or statistic features by selecting a few parameters. These features would be utilized as a pulse density modulator or a random number generator for stochastic network or Boltzmann machine.

Furthermore, novel neural network architecture utilizing chaos[5] would be realized by this simple circuit. Further analysis is being continued.

6 Conclusion

Chaotic response of the capacitance-npn-transistor pair was proved. This circuit is very simple and can be implemented by typical BiCMOS process, yet its characteristics contains many functions and is easily controllable. We simulated characteristics of the neuron circuit using this circuit in detail. The simulated results shows the feasibility to realize a novel information processing system such as chaotic neural networks.

References

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