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Does a Low Thermal Budget Help Us? -Crystallization, SiO_2 and TFT-

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Essential technologies of crystallization and SiO_2 formation are discussed for fabrication of polycrystalline silicon thin film transistors (poly-Si TFTs) at a low temperature. Polycrystalline films with fine grains (<100 nm) are formed on glass substrate via the liquid/solid interface controlled growth caused by a pulsed excimer laser irradiation. Large grain growth (>1 mm) is also discussed. Methods of remote plasma chemical vapor deposition and reactive evaporation of SiO were developed to form a SiO_2/Si interface with a low trapping density $\sim 10^{10}$ cm^{-2}eV^{-1}. These technologies realized the fabrication of poly-Si TFTs with a high mobility of 620 cm^2/Vs (n-channel) and 400 cm^2/Vs (p-channel) at 300 ^{o}C.

1. Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) are getting important for many electrical device applications, especially for liquid crystal display (LCD) and static random access memories (SRAM) applications because they have a high drive currents and both n- and p-channel TFTs are realized [1-4]. Switching elements of active matrix and integrated drive circuits can be fabricated on a same substrate. However, fabrication technology of poly-Si TFTs is less mature than that of the amorphous silicon TFT technology. New technologies are required for TFT fabrication at a low temperature and a low cost to realize devices on large area substrates.

This paper reviews methods of crystallization of silicon films using pulsed laser irradiation and formation of SiO_2/poly-Si interface at a low temperature. Fabrication process of poly-Si TFTs is also discussed.

2. Processing and Materials

2.1 Crystallization

Pulsed excimer laser heating methods have been developed to make crystalline silicon films at a low temperature [5-7]. The irradiation realizes crystallization of silicon films and activation of dopant without heating substrates to a high temperature. A liquid/solid interface is formed in thin silicon films formed on glass substrates when they are irradiated with a laser with an energy above the melting threshold, which is 160 mJ/cm^2 if the pulse width is 30ns [8]. The required energy for melting silicon films is quite low because the region heated during irradiation is limited in near surface region in depth about 1 mm because of a short heat diffusion length in the case of glass substrate. Crystallization occurs along the interface movement to the surface after irradiation through heat diffusion into the substrate (interface controlled growth). The speed of the interface was experimentally determined as 0.6 m/s [8]. The crystalline grain size increases as the laser energy increases because the melt duration increases. But the melt duration is still short at most 100 ns if the pulse width is short ~30 ns and the film thickness is thinner than 40 nm. The short and rapid crystallization results in a small crystalline grain (<100 nm) with a random orientation. Few defects like dislocations are observed in grains. Grain boundaries are formed well defined; there is no serious disordering regions. These are typical characteristics of laser crystallized films. Hydrogenation is effective to reduce defect states [9]. But the density of defect states of poly-Si films is still higher than that of hydrogenated amorphous silicon ($\sim 10^{15}$ cm^{-3}eV^{-1}) [10]. Research is still necessary to reduce defects in poly-Si films to reduce leakage current of TFTs.

Crystallization of silicon films over a large area (>30 x 30 cm^2 has been already achieved with equipments of an optical stage for scanning a laser beam with a large and stable energy whose distribution is made uniform by a homogenizer. Irradiation condition, especially for overlapping irradiation with multi pulse, has been investigated to get uniform crystalline films [11].

On the other hand, large grain growth (>1 mm) to the lateral direction has been also studied using a pulsed laser. Kuriyama *et al.* made crystalline films with large grains (111) oriented using hundred laser pulses with a help of substrate heating (~400 ^{o}C)[12]. Im *et al.* [13] reported a rapid lateral grain growth by a single pulse irradiation with an energy just below the amorphization threshold energy [14] without heating the substrate. Choi *et al.* enhanced lateral grain growth by reducing heat diffusion into the vertical direction[15]. Sameshima also realized a grain growth by inducing temperature gradient in the lateral direction by changing a shape of molten silicon islands [16]. These might be useful techniques for fabricating TFTs which have no grain boundary in the channel region.

2.2 SiO_2 formation

Formation of SiO_2 gate insulator with low damage is quite important for fabricating TFTs because defect reduction via thermal relaxation is not allowed in a low temperature process. Normal radio-frequency-induced plasma has ions and electrons with high energies 20~200 eV, which can cause serious damage into silicon. A high density of interface trapping states results in a high threshold voltage and a low carrier mobility. Serikawa *et al.* reported that a good SiO_2 formation at a temperature ~200 ^oC using a sputtering method with a O_2 gas and fabrication of poly-Si TFTs with a high mobility of 380 cm^2/Vs at 650 ^oC [17]. Kim et al. have reported SiO_2 formation with a low density of interface states ~10^{10} $cm^{-2}eV^{-1}$ using remote plasma chemical vapor deposition (CVD) below 300 ^oC [18]. Electron cyclotron resonance CVD and low pressure thermal CVDs are also attractive [19,20]. We achieved the formation of SiO_2/Si interface with the trapping density of $2x10^{10}$ $cm^{-2}eV^{-1}$ using remote plasma CVD with mesh electrodes to confine plasma as well as using SiO evaporation in an oxygen ambient [21,22]. In the remote plasma case, the mesh electrodes were used between a top electrode and a substrate in order to confine plasma. The electron density was reduced lower than 10^4 cm^{-3} near the substrate, while it was higher than 10^9 cm^{-3} in the plasma region between the tope electrode and the meshes [23]. The uniformity of SiO_2 thickness was ±1 % in 4 inch wafer. The remote plasma system will be suitable for film formation with low plasma damage over the large area. The method of SiO evaporation in an oxygen ambient is also attractive for film formation at a low temperature. Evaporated SiO molecules efficiently react with an oxygen gas so that SiO_2 can be formed without a help of plasma. The simple system would be helpful for a fabrication process.

However, SiO_2 films formed by these methods do not have same properties as thermal oxidized SiO_2, which is in complete thermal relaxed state [24]. O-H and weak Si-O bondings are contained in the films. They can cause defects like positive charges trapped states and leakage currents. Sano *et al.* reported that a post-deposition annealing in wet atmosphere made the films more stable and to reduce defects at the interface as well as in SiO_2 at a temperature below 300 ^oC [25]. Such chemical process will be useful to overcome problems low-temperature SiO_2 has. Further research is necessary for improving stability as well as interface properties.

3. TFT Fabrication and results

Many reports have already demonstrated that TFTs with a high mobility are fabricated using laser crystallization of silicon films [5,6,12,15,17,26,27]. Moreover, some integrated circuits have been fabricated with TFTs [28-30]. However, fabrication technology of poly-Si TFTs is less mature. The author believes that development of equipments is one of most important point to establish a fabrication process for good TFTs. Figure 1 shows a schematic of our fabrication apparatus containing multi chamber. Undoped and doped silicon films were crystallized with laser irradiation in vacuum. The plasma hydrogenation was carried out to reduce defects in crystallized silicon just after crystallization. Then SiO_2 was deposited on the silicon films as a gate insulator. The multi-chamber system shown in Fig.1 kept samples clean in vacuum and a same temperature among these process steps. It is useful to realize a rapid fabrication with a high yield.

Figure 2 shows transfer characteristics of n-channel poly-Si TFTs fabricated at 300 ^oC [21,22]. The maximum field effect mobility and the minimum threshold voltage was 620 cm^2/Vs and 0.8 V, respectively. P-channel TFTs were also fabricated. The mobility and the threshold voltage were 400 cm^2/Vs and -1.5 V, respectively. These results show that TFT fabricated at a low temperature can have good characteristics. The minimum defect density in TFTs was estimated to be about $2x10^{11}$ $cm^{-2}eV^{-1}$ from the results of Fig.2, which was higher than the minimum interface trapping density obtained from C-V characteristics of MOS capacitors. There must be still defects in SiO_2, poly-Si and at the interfaces of SiO_2/poly-Si and poly-Si/underlying substrate. The variation of the threshold voltage was ±0.4 V in our fabrication. Variation of the threshold voltage reduces the speed operation of an integrated circuit in a low operation voltage. Reduction of defects is essential to realize reliable performances.

4. Summary

The method of pulsed laser melt-regrowth results in formation of polycrystalline silicon films with fine crystalline grains (<100 nm) on a glass substrate at a low processing temperature. Large grain growth (>1 mm) is also possible by causing grain growth in the lateral direction. SiO_2 formation is one of essential steps for fabrication of TFTs. n-channel and p-channel poly-Si TFTs were fabricated at 300 ^oC using technologies of laser crystallization and methods of SiO_2 formation in remote plasma chemical vapor deposition or SiO evaporation in an oxygen ambient. The maximum field effect mobility was 620 cm^2/Vs for poly-Si TFTs. These results demonstrate that TFT can have good performances by forming SiO_2 gate insulator with low damage.

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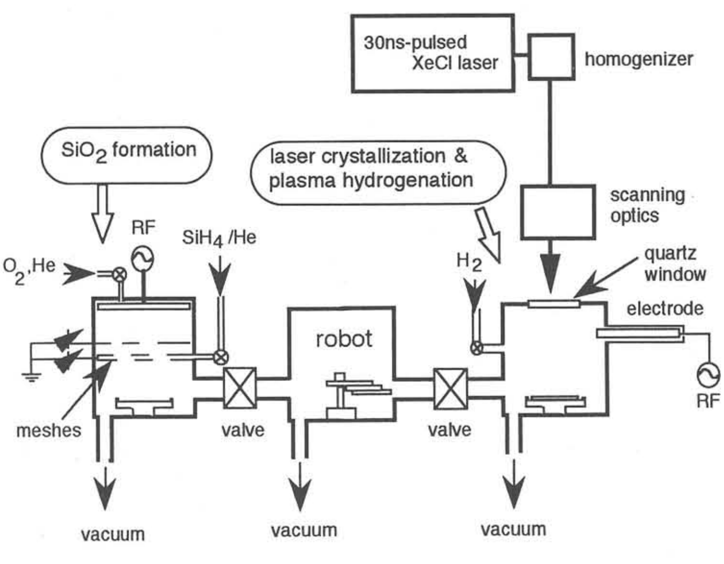

Fig.1 Schematic apparatus with equipments for crystallization, hydrogenation, SiO_2 formation and wafer transfer in vacuum.

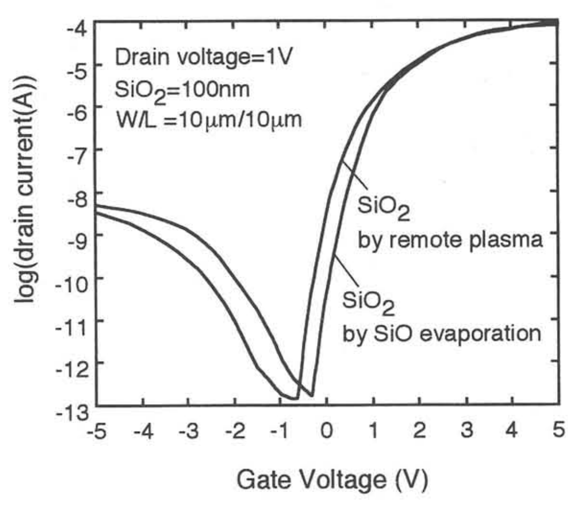

Fig.2 Transfer characterisitcs for n-channel TFTs. SiO_2 gate insulators were formed with remote plasma CVD as well as SiO evaporation.