

Impact of μ A-ON-Current Gate All-Around TFT (GAT) for 16MSRAM and Beyond

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A Gate All-around TFT (GAT) with thin channel poly-Si can exhibit suppression of performance fluctuation induced by poly-Si grain boundary in the channel in addition to the improvement of the average performance compared to the Single-Gate TFT (SGT). This effect is due to the thinning of effective channel poly-Si by half for the GAT. Poly-Si TFT simulation clearly supported this effect on the I-V characteristic and channel potential. The GAT with sacrifice oxidation also reduce the -BT stress instability because the double-gate relaxes the stress of electric field in the gate oxide. The high performance GAT can shrink the SRAM cell owing to providing high ON-current to the storage node and raising the data hold stability in spite of the poor cell ratio. The GAT-SRAM cell is a strong candidate for the 16MSRAM and beyond.

1. INTRODUCTION

For large scale integrated SRAMs such as 4M bit and beyond, TFT load has been become necessary for cell performance of low power consumption and data retention. The poly-Si TFT exhibits inferior performance, so that SRAM cell with TFT-loads requires large cell ratio. Therefore, it results in the large cell size for achieving large cell ratio. This problem has been becoming a serious obstruction to the integration of TFT-load SRAM. The solution of the problem is obtaining high performance TFT's. The grain size enlargement is one of the technology to improve the average performance of TFT¹⁾. However, it increases the fluctuation of TFT performance caused by the variation of poly-Si grain boundary length in the channel²⁾. As a countermeasure, the control technique of poly-Si grain position in the TFT has been proposed³⁾, but its process can not be actually applied to the LSI process. Another technique for the performance improvement is the structural innovation. The double-gate

TFT exhibits higher average performance than the single-gate one owing to the increase of gate controllability⁴⁾. This improvement would be observed for every TFT in an SRAM chip and has a good effect on the suppression of the performance fluctuation. Recently, we proposed the GAT which provides high average ON-current and of which fabrication process is simpler than the double-gate TFT in spite of almost the same gate structure as the double-gate one⁵⁾.

In this paper, a novel GAT-SRAM which has small cell ratio and small cell size is introduced. The GAT provides μ A-ON-current and enables us to reduce the cell size. Furthermore, GAT improves the TFT reliability which is becoming a grave problem in TFT with thinner gate oxide.

2. DEVICE FABRICATION

The GAT structure is illustrated in Fig.1(a). Its fabrication process using dummy nitride pattern and its removing requires only one ad-

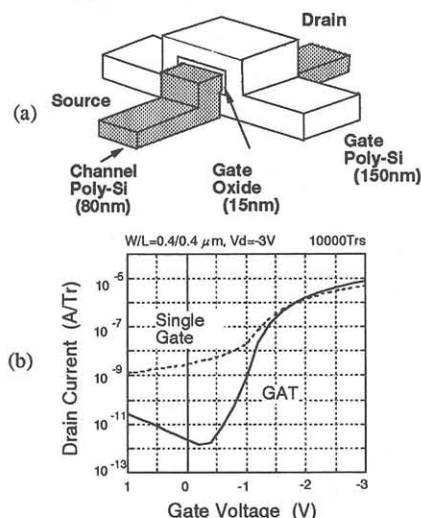


Fig.1 Gate All-Around TFT (GAT). (a) GAT structure, (b) average I_d - V_g characteristics of SGT and GAT. (Ref.(5))

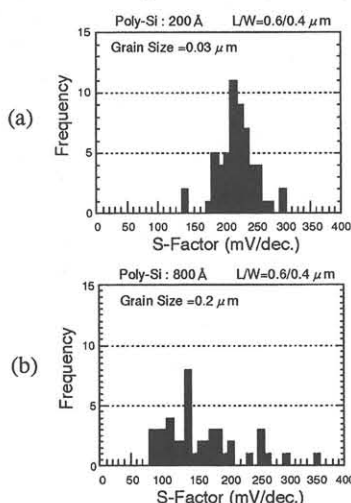


Fig.2 Comparison of S-Factor fluctuation in conventional single-gate TFT (SGT). (a) Grain size of channel poly-Si is 0.03 μ m, (b) 0.2 μ m.

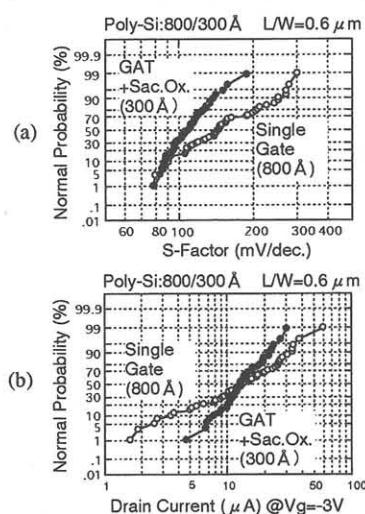


Fig.3 Fluctuation comparison in SGT and GAT with sacrifice oxidation. (a) S-Factor, (b) drain current. The GAT suppresses the both of fluctuation.

ditional mask layer to the SGT process⁹. The channel poly-Si layer was obtained from a-Si deposition and its crystallization. The thickness of channel poly-Si was varied from 20 to 80 nm and that of the gate oxide and gate poly-Si were 15, 150 nm, respectively. The sacrifice oxidation of channel poly-Si was applied to 80 nm poly-Si, where the poly-Si was thinned from 80 nm to 30 nm thick. For comparison, we also fabricated top-gate TFT's as SGT. Both TFT's were p-channel type and the gate length is 0.4 μ m. -BT stress was examined, where the gate bias to source and drain was -5V and temperature was 125 $^{\circ}$ C.

3. RESULTS AND DISCUSSION

a. Analysis of TFT Characteristic Fluctuation

Fig.2 shows comparison of S-factor fluctuation in conventional SGT's with poly-Si having grain size of 0.03 μ m (Fig.2(a)) and 0.2 μ m (Fig.2(b)). These graphs imply that the grain size enlargement increases the fluctuation of S-factor in spite of the improvement of average S-factor. It is considered that the S-factor fluctuation is caused by the presence probability of poly-Si grain boundary in the channel region and the grain size variation. Fig.1 depicts the structure of GAT and its superior average characteristics compared to SGT⁹. The GAT can raise the average ON-current and suppress the short channel effect such as the punch-through resulting from gate all-around effect. Fig.3 shows fluctuation comparison of S-factor (a) and drain current (b) in the SGT and the GAT with the sacrifice oxidation of channel poly-Si. The GAT with the sacrifice oxidation exhibits the suppression of the both fluctuations and provides μ A-order ON-current. In order to clarify the suppression mechanism in the GAT, we made a comparison between the performance fluctuation of TFT with 80 nm and 20 nm-thick poly-Si, as shown in Fig.4. The GAT with thinner channel poly-Si suppresses the performance fluctuation. It is considered that a coupling of the double gates in the channel eliminates the performance degradation caused by the grain boundary and improves the poor performance of the TFT with the grain boundary in the channel. The performance improvement by the GAT structure in the TFT which has the grain boundaries in the channel is thought to be greater than that of the TFT with no grain boundary in the channel. As a result, the reduction of performance fluctuation can be obtained.

In order to clarify a mechanism of the above experimental results, we simulated the electrical characteristics in TFT using the home-made device simulator modified for poly-Si TFT. Fig.5 shows simulated Id-Vg characteristics for the SGT and GAT as a parameter of the trap density at a grain boundary, which exists at the center of the channel. The channel poly-Si thickness is 30 nm, so that the channel poly-Si is fully depleted. The S-factor is degraded as the trap-state density increases in the SGT and GAT, but the degradation in the

GAT is smaller than that in the SGT. In addition to the experimental result, the simulation result also suggests that the GAT structure suppresses the S-factor fluctuation caused by the grain boundary traps. This suppression is qualitatively elucidated by thinning of the effective poly-Si thickness for case of full-depleted channel in the equations as given in Fig.5. S-factor is determined by the total trap state density which linearly depends on poly-Si thickness. Therefore, the poly-Si thinning by the double-gate effect improves the S-factor owing to the reduction of the effective trap state density. Fig.6 showed simulated potential distributions at grain boundary in channel poly-Si in the lateral direction for the SGT and GAT. The GAT can lower the height of potential barrier which is generated at the grain boundary and impedes carrier mobility. Fig.7 shows measured data of potential barrier height in the channel which was obtained by the temperature dependence of the drain current. The barrier height reduction is also observed for the GAT compared to the SGT and this result verifies the above simulation result.

b. Reliability improvement

-BT stress was reported to be a serious problem in the reliability for the TFT¹⁰, so that we examined the stress immunity for the GAT. Fig.8 shows Vth shift caused by -BT stress for the SGT and GAT. The GAT structure and sacrifice oxidation of poly-Si can extend the stress life time by a factor of three. In order to investigate this mechanism, we simulated the electrostatic potential of the TFT under the -BT stress. Fig.9 illustrates the simulation result of vertical potential distribution at the grain boundary in the GAT and SGT. The GAT structure relaxes the electric field in gate oxide and this brings about the reliability improvement. This relaxation is attributed by the decrease of the effective depletion charge in the channel poly-Si caused by the double gate.

c. Proposal of GAT-SRAM

We studied influence of μ A-ON-current TFT on SRAM cell performance. Fig.10 shows transfer curves in the SRAM cell with poor cell ratio of 1.38. As compared to case of no supply current by TFT (Fig.10(a)), static noise margin is improved by the TFT providing 2 μ A. Therefore, high performance TFT does not require high cell ratio and can contribute to the cell size reduction. Fig.11 depicts a proposed cell layout designed on a 0.3 μ m rule. Cell area and TFT L/W is equal to 3.93 μ m² and 0.4/0.3 μ m, respectively. Small SRAM cell can be obtained by utilizing the sub-half micron channel GAT exhibiting high performance as a load device.

4. CONCLUSION

We found the suppression of performance fluctuation for the GAT. The S-factor degradation by the poly-Si grain boundary is reduced by the GAT structure with thin channel poly-Si. The

mechanism was investigated using the poly-Si TFT simulation on the I-V characteristics and channel potential. We demonstrated that the GAT exhibits high -BT stress immunity. This is because the GAT structure relaxes the stress electric field in the gate oxide on the grain boundary owing to the double-gate effect. Small cell size ($3.93 \mu\text{m}^2$) for SRAM was proposed utilizing the GAT as a load device. Cell size reduction is due to the short channel GAT and small cell ratio. The GAT-SRAM with simple process, high reliability and small cell size is attractive candidate for 16MSRAM and beyond.

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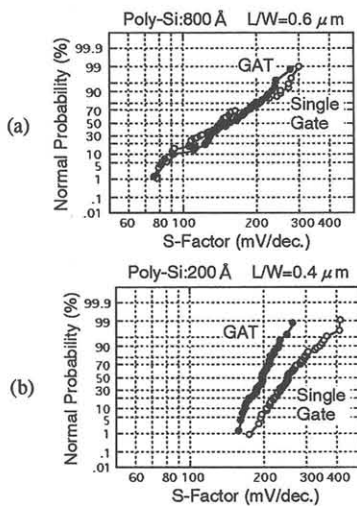


Fig.4 Fluctuation comparison of S-Factor in SGT and GAT. (a) with 800 Å poly-Si, (b) 200 Å poly-Si. The GAT with thinner channel poly-Si reveals suppression of performance fluctuation.

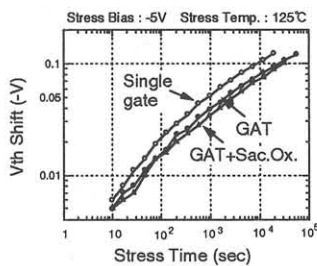


Fig.8 V_{th} shift caused by -BT stress. GAT and sacrifice oxidation of poly-Si extend stress life time by a factor of three.

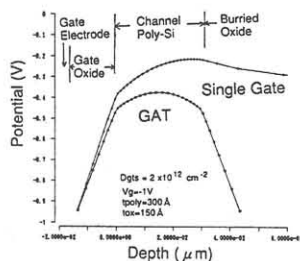
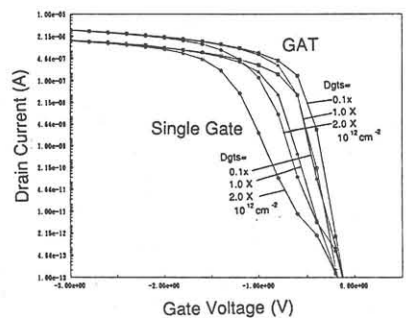


Fig.9 Simulated potential distribution in vertical direction at poly-Si grain boundary in GAT and SGT.



$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{Cd + qDit + qDgt}{Cox} \right)$$

$$Dgt \propto Dgts \times t_{poly}$$

$Dgts$: trap density at grain boundary surface
 Dgt : trap density of grain boundary in unit channel area
 t_{poly} : channel poly-Si thickness
 Dit : trap density at poly-Si/SiO₂ interface
 Cd : capacity of depletion layer
 Cox : capacity of gate oxide

Fig.5 Simulated I_d - V_g characteristics in SGT and GAT as a parameter of trap density at grain boundary. Poly-Si TFT simulation also shows the suppression of S-Factor fluctuation due to GAT. This suppression is qualitatively elucidated by reduction of poly-Si thickness in the equations.

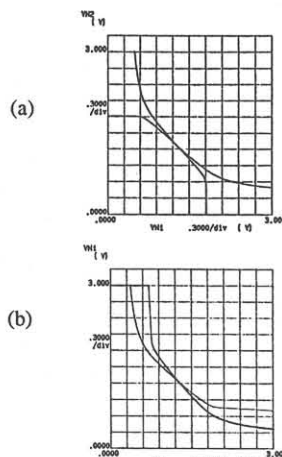


Fig.10 Transfer curves in the SRAM cell with cell ratio of 1.38. (a) No supply current by TFT, (b) TFT provides $2 \mu\text{A}$.

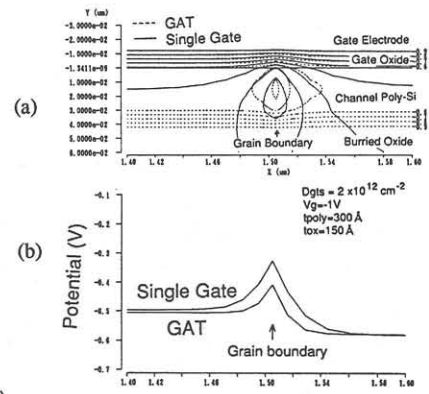


Fig.6 Simulated potential distribution at grain boundary in channel poly-Si for SGT and GAT. (a) contour map of electric potential, (b) potential barrier in lateral direction.

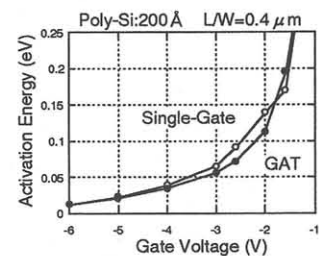


Fig.7 Measured data of potential barrier height in the channel. This verifies the above simulation.

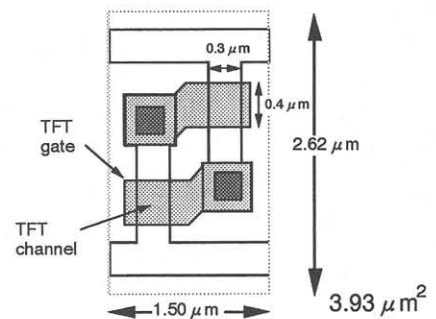


Fig.11 Proposed cell layout designed on a $0.3 \mu\text{m}$ rule. Cell area and TFT L/W is equal to $3.93 \mu\text{m}^2$ and $0.4/0.3 \mu\text{m}$, respectively. Small SRAM cell is obtained by GAT.