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PMOS Thin-Film Transistors Fabricated in RTCVD Polycrystalline Silicon Germanium Films

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PMOS thin film transistors(TFTs) have been fabricated in rapid thermal chemical vapor deposition (RTCVD) polycrystalline silicon-germanium(poly-$Si_{0.82}Ge_{0.18}$) films for the first time. The transistors with channel length down to 1.5 μm exhibit to be well-behaved in electrical characteristics. The device performance was degraded in proportion to oxygen content which was measured by secondary ion mass spectrometry(SIMS). After electron cyclotron resonance(ECR) plasma hydrogenation at optimal conditions, trap density of states decreased remarkably, which resulted in lower leakage current($\sim$1.4pA/μm) and higher field-effect hole mobility($\sim$7.4cm^2/V.sec).

1. INTRODUCTION

In recent years, polycrystalline silicon(Poly-Si) thin film transistors(TFTs) are widely used in large-area electronics applications including linear image sensors and liquid crystal displays(LCDs) with integrated peripheral circuits. Low temperature process and short process times are essential for reducing the manufacturing cost. The thermal budget for high performance poly-Si TFT process is so tight that inexpensive glass substrates can not be adapted because of glass warpage and shrinkage with high temperature. This problem can be relaxed by using the poly-$Si_{1-x}Ge_x$ films which can be deposited and crystallized at lower temperature, which leads to lower thermal budget process as compared to the poly-Si TFTs.[1] In RTCVD, the process temperature is used in place of gas flows to initiate and terminate chemical reactions on wafer surfaces, which can be heated to the process temperature in few seconds. As a result, ultra-thin films with short time processing can be obtained by this techniques.[2] In this work, poly-$Si_{1-x}Ge_x$ films deposited in RTCVD system are investigated by analysis tools(X-ray diffraction(XRD), Auger electron spectroscopy(AES), and SIMS) and evaluated by electrical characteristics.

2. DEVICE FABRICATION

The device structure of this work is a self-aligned top gate PMOS as shown in Fig-1. The poly-$Si_{1-x}Ge_x$ films were deposited on oxidized 4-inch silicon wafer by using RTCVD system at 700°C to the thickness of about 2800Å which were processed under condition that gas flows of GeH_4 and SiH_4 are 5 sccm and 10 sccm respectively with the actual process pressure of 10 torr. In Fig-2, several singular peaks show the characteristics of polycrystalline material with diamond crystal structure as a result of XRD analysis. This poly-$Si_{1-x}Ge_x$ films have more or less strong grain texture of (220) grain orientation. Germanium mole fraction of deposited poly-$Si_{1-x}Ge_x$ film is estimated to be about 0.18 with AES analysis. Active patterns were defined by reactive ion etch(RIE) typed plasma etching with SF_6 and CCl_2F_2 gas mixture and 1000Å-gate oxide film was deposited by APCVD. Poly-Si films for gate electrode were deposited to the thickness of 3500Å by LPCVD and $POCl_3$ doping was carried out subsequently. After patterning the gate poly-Si and BF_2 ion implantation, anneal process(600°C,60 min.) was followed. 3000Å-interlayer oxide was deposited by APCVD and contact patterning & Al-Si metallization were processed sequentially. Metal alloy was also processed at 400°C for 30 minutes. After initial measurements of the I-V characteristics and SIMS analysis were made, hydrogenation of PMOS poly-$Si_{1-x}Ge_x$ TFTs was performed by ECR plasma hydrogen treatments with various times at 400°C. The process pressure and microwave power are about 0.3 mTorr and 600 W. After that process, the devices were subsequently measured again.

3. RESULTS AND DISCUSSION

Before hydrogenation, oxygen content of poly-$Si_{0.82}Ge_{0.18}$ TFTs with different electrical characteristics were analyzed by SIMS. Grain nucleation ratio and grain growth rate during the crystallization anneal may have been retarded in accordance with higher oxygen content which will be resulted in small grain

sizes of poly-$Si_{1-x}Ge_x$ film.[3] Fig-3 shows that the oxygen content in poly-$Si_{0.82}Ge_{0.18}$ channel layer has strong relations with the electrical properties such as hole mobility and inverse subthreshold slope which was affected by a density of trap states.[4] Typical Vg-Id curves and Vd-Id curves are shown in Fig-4 and Fig-5 for a small transistor(W=L=1.5μm) before and after 40 minute ECR plasma hydrogen treatment. Fig-4 indicates that the reduction rate of off-state current is much higher than the increasing rate of on-state current after hydrogenation. It is known that on-state current is closely related to tail-state density near band edges in the bandgap and off-state current suppression is attributed to the reduction of deep-state density around the midgap although orthodox is not fixed.[5] In this point of view, poly-$Si_{0.82}Ge_{0.18}$ TFTs especially in small gate length devices have been improved significantly on trap density of states by ECR plasma hydrogen treatment. All electrical parameters are summarized in Table-1. The maximum ON/OFF current ratio with off-current level of 0.3 pA was 8.35×10^6 at which $Vds = -1.0V$. Field effect mobility was calculated in linear region at maximum transconductance. In this poly-$Si_{0.82}Ge_{0.18}$ TFT films, it seems that it's hard to enhance the field effect mobility to a large extent due to the higher oxygen and carbon content (It's about 3 percents to each as a result of AES measurement) which causes the films to be more small grain sizes and to increase surface roughness.[6] Low field effect hole mobility results from the surface scattering of the active channel and a higher trap density of states. From the characteristics curve shown in Fig-5, it is apparent that short channel effects can be seen only a little even for a small transistor. The duration of hydrogenation determines electrical characteristics of different channel sizes in Fig-6 and Fig-7. These figures suggest that there exists the saturation condition of hydrogen passivation at the given device structure. It was observed that no device degradation could be measured, preferably with a slight increase of device performance even through excess hydrogenation (more than saturation time of hydrogen passivation) was applied to poly-$Si_{0.82}Ge_{0.18}$ TFTs. The lateral hydrogen diffusivity by a simple relation of diffusion length $\sqrt{Dt}$ at 400°C can be calculated at about 8.0×10^{-12}cm^2/sec in this structure from Fig-6. The difference of electrical characteristics in short- and long-channel devices after hydrogenation indicates that there exist two types of hydrogen diffusion path(vertical and lateral paths) and also indicates that short-channel devices were more efficiently passivated than long-channel ones.[7]

4. CONCLUSION

PMOS TFTs with poly-$Si_{0.82}Ge_{0.18}$ films deposited by RTCVD system have been fabricated and evaluated for the first time. The device performance was degraded in proportion to oxygen content in poly-$Si_{0.82}Ge_{0.18}$ channel layer. The electrical properties of this device were significantly improved especially in short-channel devices with ECR plasma hydrogenation.

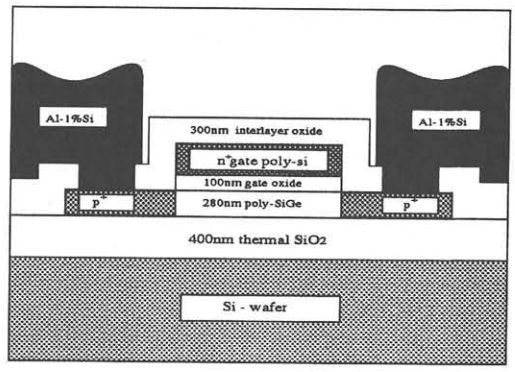

Fig-1. Cross-sectional view of a PMOS thin-film transistor.

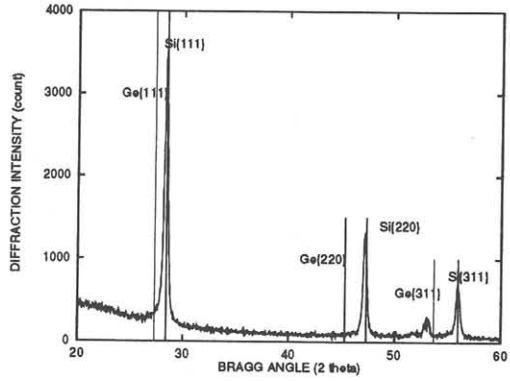

Fig-2. XRD data of poly-$Si_{0.82}Ge_{0.18}$ film deposited in RTCVD system.

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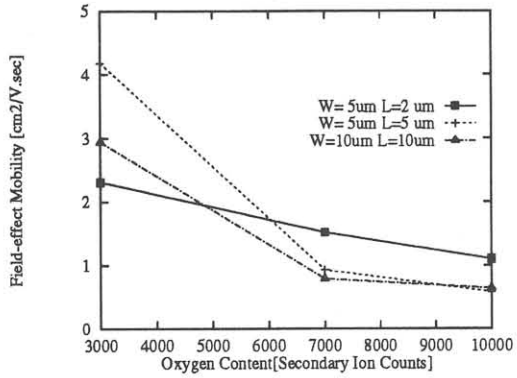

Fig-3. Channel oxygen content(from SIMS analysis data) versus field-effect hole mobility plot.(No Hydrogen Passivation)

Electrical Performance Parameter Summary

Electrical Parameters	No Hydrogenation.	ECR Plasma Hydrogenation
Threshold voltage(V)	- 6.6	-2.5
Field effect mobility(cm ^{2}/V.s)	4.4	7.4
Subthreshold slope(V/dec)	3.1	0.6
Leakage currrent(pA/um)	713.3	1.4
Maximum I_{ON} / I_{OFF}	1.5E4	1.3E7

W/L = 1.5 um/1.5 um Vd=-5.0V

Table-I. Electrical performance parameters of PMOS poly-$Si_{0.82}Ge_{0.18}$ TFTs. The threshold voltage is determined by Vg versus $\sqrt{Id}$ curve at which Vd=Vg.

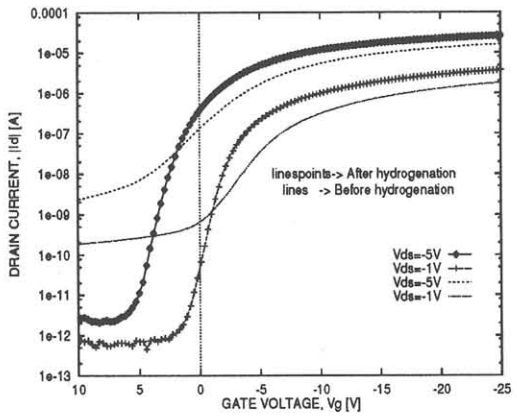

Fig-4. Subthreshold characteristics of RTCVD poly-$Si_{0.82}Ge_{0.18}$ TFT at which W=L=1.5μm in layout.

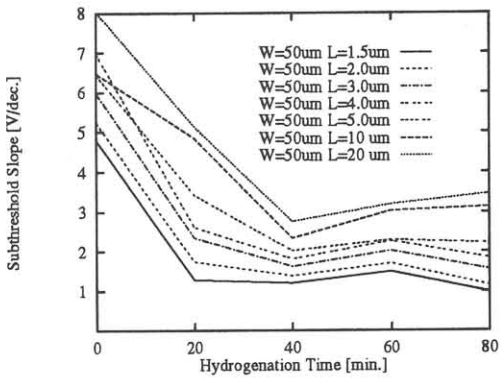

Fig-6. Subthreshold slope versus hydrogenation time plot at which Vd=-1.0 V.

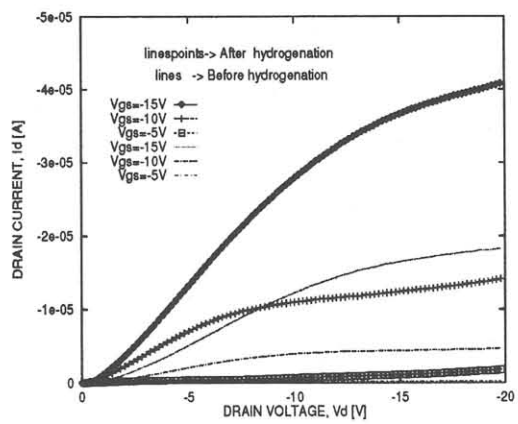

Fig-5. Measured Vd-Id characteristics of PMOS poly-$Si_{0.82}Ge_{0.18}$ TFTs at which W=L=1.5μm.

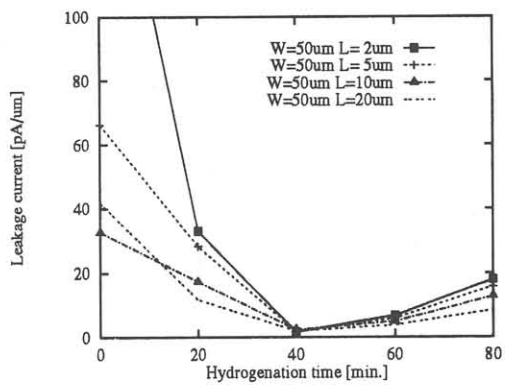

Fig-7. Leakage current is shown with a function of hydrogen passivation time for W=50μm, L=2μm, 5μm, 10μm 20μm respectively at which Vd=-1.0 V.