Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 809-811



# Analysis of Structure-Dependent Hot Carrier Effect in Various LDD MOSFET's Using an Efficient Interface State Profiling Method

*J.-J. Yang, Steve S. Chung, P.-C. Chou, J.-R. Shih*, C.-H. Chen* and M.-S. Lin**

*Department of Electronic Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.*
** Taiwan Semiconductor Manufacturing Co., Hsinchu Science-Based Park, Taiwan, R.O.C.*

To investigate the device degradation process in more detail, it is mandatory to physically characterize the interface state distribution. In this paper, a new and efficient interface state profiling technique suitable for submicron MOSFET drain-engineering study was proposed to investigate the structure-dependent hot carrier effect. The shape of interface state profile is found to be similar to that of the surface electric field. We found that for conventional LDD device, sidewall spacer is the dominant damaged region, which gives direct evidence of spacer-induced degradation. LATID device has better hot carrier reliability since interface states are spreaded over the wide gate/drain overlapped region and the associated series resistance effect is weaker than that of conventional LDD devices.

## 1. Introduction

To compare and understand the hot carrier effect of drain-engineered MOSFET's, such as LDD, MLDD[1], and LATID[2] devices, the commonly used substrate current ($I_B$) or total amount of generated interface states is not a sufficient criterion. For these devices, the hot carrier induced drain current ($I_D$) degradations ($\Delta I_D/I_{D0}$) are closely related to the position of generated interface states ($N_{it}$) and device parameters such as $n^-$ profile and gate oxide thickness[3]. In the past, the structure-dependent hot carrier effect was understood only using device simulation[4].

In general, the charge pumping (CP) technique for probing highly localized $N_{it}$ distribution is to correlate the decrements of CP current and the extension of depletion region at channel/drain junction by stepwisely applying a reverse bias at drain or bulk electrode[5]. Therefore, this approach is not appropriate and efficient for applying to MOSFET's with graded channel/drain junction especially for drain-engineered MOSFET's since the depletion width needed to be calculated by device simulation or analytical formulae which will greatly limit the profiling accuracy. In this paper, an improved CP method based on our reported method[6] to reliably characterize the spatial $N_{it}$ profile is first developed. A 2-D device simulator is used to verify the validity of the current approach. The influence of tailing device drain doping profile on the distribution of hot carrier induced interface states, the correlation between the interface state profile and the device degradation will then be studied.

Three typical drain-engineered MOSFET's that cover essential design concepts for lightly doped drain structure, named as LDD, MLDD and 45° LATID devices, were studied. Table 1 lists the gate oxide thickness ($T_{ox}$) and $n^-$ implantation conditions for each device. The 45° LATID device has $n^-$ region that was performed by a 45° tilt angle phosphorus implantation. Several device parameters are also listed in Table 1 to help getting insight into device characteristics. Each device was stressed at $V_{DS}=2V_{GS}=7V$ for hot carrier effect comparison .

## 2. A New Interface State Profiling Method

The experimental setup for the fixed base level *CP measurement* is shown in Fig. 1. The source, drain and bulk electrodes of tested device are grounded. After appropriate physical and mathematical manipulations, the lateral distribution of generated $N_{it}$ ($\Delta N_{it}(x)$, in unit $cm^{-2}$) can be expressed as

$$\Delta N_{it}(x)=f\cdot q\cdot W\cdot\frac{d\Delta I_{CP}(V_{gh})}{dV_{gh}}\cdot\frac{dV_{gh}}{dx}, \qquad (1)$$

in which, f is the gate pulse frequency, W is device channel width, and x is the channel position. Since increasing $V_{gh}$ widens the lateral detectable damaged region toward the channel direction, indeed, the $V_{gh}$ versus detected length relationship implies the spectroscopy of local threshold voltage $V_{th}$. In other words, $V_{gh}$-x relationship is identical to that of $V_{th}$-x. Calculating $dV_{th}/dx$ from 2-D device simulation and $d\Delta I_{CP}/dV_{gh}$ from measured $\Delta I_{CP}$-$V_{gh}$ curves, (1) provides us a simple and accurate way to characterize $\Delta N_{it}(x)$ from CP measurement. The current method needs not to calculate troublesome depletion width and can obtain continuous $N_{it}$ profile ranged from spacer region to the middle of the channel, which is very important for examining hot carrier effect.

Figure 2 gives the simulated $V_{th}$-x relationship. Fig. 3 shows the characterized time evolution of $\Delta N_{it}(x)$ for the device LDD. The validity of present method to characterize $\Delta N_{it}(x)$ is verified by Minimos which shows pretty good agreements as shown in Fig. 4 by a comparison with the experimental data. In Fig. 3, the peak position of $\Delta N_{it}(x)$ is separated from those of $E_x$ and hot carrier injection current by 150Å. Advanced device simulation proved that this discrepancy is very reasonable due to the non-local effect in submicron MOSFET's since carriers need to travel sufficient distance to become energetic. Fig. 5 compares the $N_{it}$ profiles for the MLDD, 45° LATID and LDD devices after 11000 seconds stress. Positions A, B, and C are the channel/$n^-$ junction for the devices MLDD, LATID and LDD, respectively. Although the current profiling technique does need not the information of surface electric field, the characterized $N_{it}$ profile is found to be similar to the shape of surface electric field, which validly supports the appropriateness of the $N_{it}$ profiles. The damaged region can be splitted into three regions as illustrated in Fig.1 for studying device degradation mechanisms. Region I is the channel region, Region II is the gate/drain overlapped region and Region III is the spacer region.

## 3. Structure-Dependent Hot Carrier Effect in Device Drain Engineering

Figure 6 compares time evolutions of $I_{CP}$ increment and $\Delta I_D/I_{D0}$ (evaluated at $V_{GS}$=5V and $V_{DS}$=0.1V) during hot carrier stress for the studied devices. Although LDD has the minimum $\Delta I_{CP}$ value, its $\Delta I_D/I_{D0}$ is the largest. Clearly, the factor $\Delta I_{CP}$ (as well as the total amount of $\Delta N_{it}$) cannot reflect the degree of the $I_D$ degradation. The results reveal that the device degradation is strongly drain structure dependent. The degradation process can be comprehensively understood by $N_{it}$ profiles shown in Fig. 5. For these devices, the peaks of $N_{it}$ profiles are all located outside the gate edge, which will introduce additional series resistance and cause the so-called spacer-induced degradation. By integrating the $\Delta N_{it}(x)$ in each damaged region, we found that the dominant damaged regions for MLDD and 45° LATID devices are Region II, for LDD device is Region III.

Figure 7(a) shows the simulated variation of device surface electron concentration before stress and after stress 11000 seconds for LDD. LDD device has the largest $N_{it}$ peak and the position of peak is located far from the gate edge as compared with others. The reduction of electron concentration in spacer region is very significant owing to its lighter $n^-$ region doping concentration, therefore, increases the series resistance in the spacer region. This series resistance effect causes the largest $I_D$ degradation for LDD devices.

In contrast to the LDD, the $n^-$ tilt implantation makes the 45° LATID device having the nature that keeps large portion of the heated carriers inside the gate edge and therefore widens the $N_{it}$ distribution. The $N_{it}$ distribution in LATID is much more flat and spreaded over the wide gate/$n^-$ overlapped region as showing in Fig. 5. Fig. 7(b) shows the simulated variations of surface electron concentration before stress and after 11000 seconds stress for LATID. Since LATID has the largest surface doping concentration as shown in Fig. 5 and the transverse electric field has more controllability to compensate the reduction of electron concentration in the gate/$n^-$ overlapped region, the hot carrier effect induces lower series resistance effect as well as the $I_D$ degradation in LATID devices.

The MLDD has the maximum $\Delta I_{CP}$ and a higher $n^-$ concentration than LDD, simulation results prove that the resistance effect is between the above two cases. By examining the $N_{it}$ profiles of MLDD and LDD, incresing $n^-$ dosage can shift the dominant damaged region toward the channel direction, which increases the gate controllability over the damaged region. This fact helps alleviating the series resistance effect in MLDD.

## 4. Conclusion

Several salient features of the newly proposed $N_{it}$ profiling method are 1) easy to implement; 2) suitable for device drain-engineering design in submicron MOSFET's; and 3) allowed us to characterize $N_{it}$ ranged from spacer region to the middle of device channel which is very important in analyzing hot carrier effect. This method was applied to study structure-dependent hot carrier effects in various LDD devices. The study successfully characterized the relationship among device drain structure, $N_{it}$ profile and the current degradation. The $N_{it}$ profile dominates the $I_D$ degradation. With a trade-off between the use of $n^-$ implantation dosage and angle, we conclude that the design optimization of a hot carrier resistant MOS device can be better understood through the use of the newly developed interface state profiling technique.

**Acknowledgements** This work is sponsored by the National Science Council under contract No. NSC82-0404-E009-377. Device fabrication by the TSMC and the support by the R&D devision are gratefully acknowledged.

## References

1) M. Kinugawa, et al., in Tech. Digest Symp. on VLSI Technology (Japan 1985) 116.
2) T. Hori, et al., in Tech. Digest Symp. on VLSI Technology (Japan 1988) 15.
3) Y. Toyoshima, et al., in Tech. Dig. IEDM (USA 1984) 786.
4) W. Hanch, et al., IEEE Trans Electron Device ED-38 (1991) 512.
5) W.-L. Chen, et al., IEEE Trans Electron Devices ED-40 (1993) 187.
6) S. S. Chung, et al., in Proc. 1993 SSDM (Japan 1993) 841.

| Group | MLDD | LATID | LDD |
|---|---|---|---|
| $T_{ox}$ (Å) | 140 | 140 | 140 |
| $n^-$ Dose ($cm^{-2}$) | $4.0\times10^{13}$ | $4.0\times10^{13}$ | $2.0\times10^{13}$ |
| Energy (keV) | 80 | 80 | 80 |
| Angle | 0° | 45° | 0° |
| $L_{mask}/L_{eff}$ | 0.7/0.51 | 0.7/0.43 | 0.7/0.64 |
| $V_T$ (V)@$V_{BS}$=0V | 0.7545 | 0.7773 | 0.7845 |
| $I_{DN}$@$V_{DS}$=$V_{GS}$=5V (mA) | 9.02 | 9.62 | 7.87 |

Table 1 The device fabrication parameters and measured device parameters.

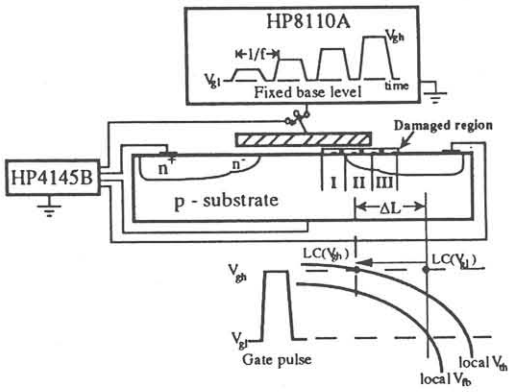


Fig. 1 Experimental setup and principles of the CP measurement.

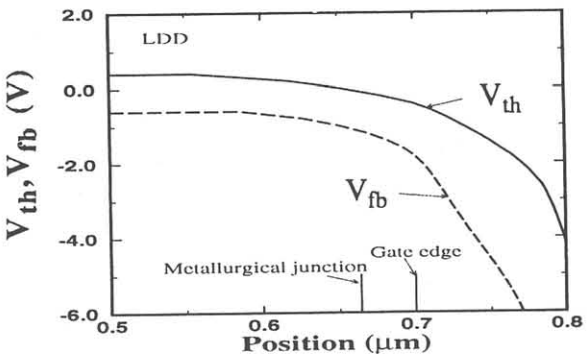


Fig. 2 The simulated local threshold voltage ($V_{th}$) and the flatband voltage ($V_{fb}$).

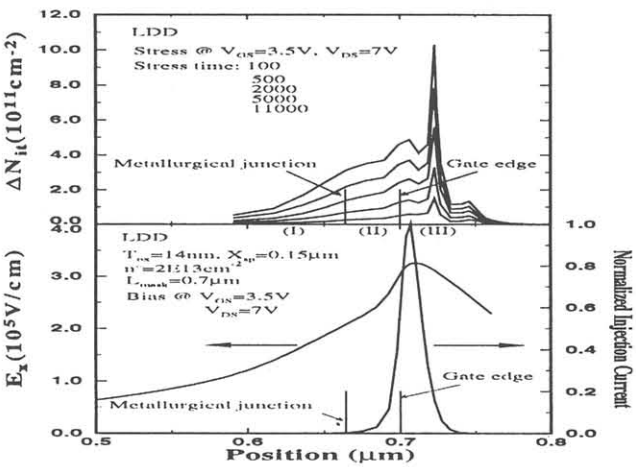


Fig. 3 Time evolution of $\Delta N_{it}$ distribution for the LDD device.

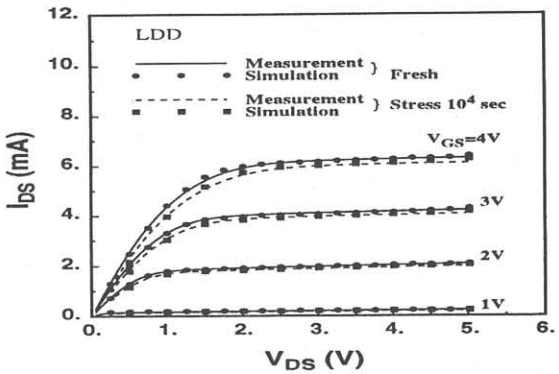


Fig.4 The verification of the $\Delta N_{it}(x)$ by 2-D simulation of drain currents.

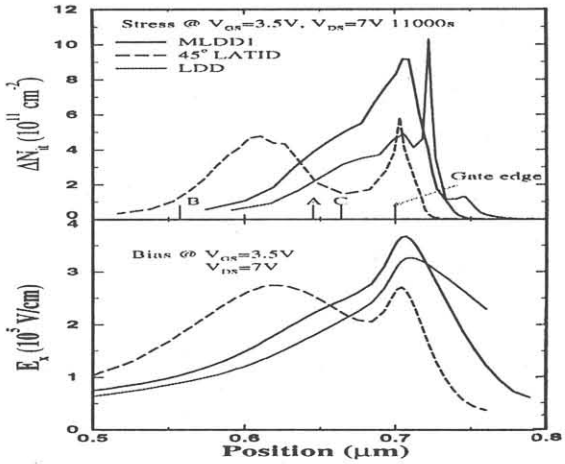


Fig. 5 Comparison of $N_{it}$ profile and surface electric field for various LDD MOSFET's.

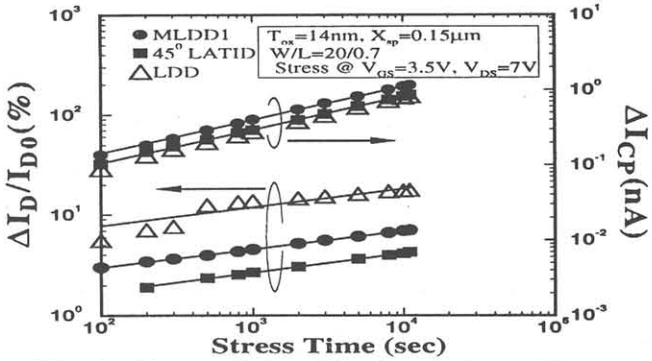


Fig. 6 Time evolution of $I_D$ degradation and $I_{CP}$ increment for various LDD MOSFET's.

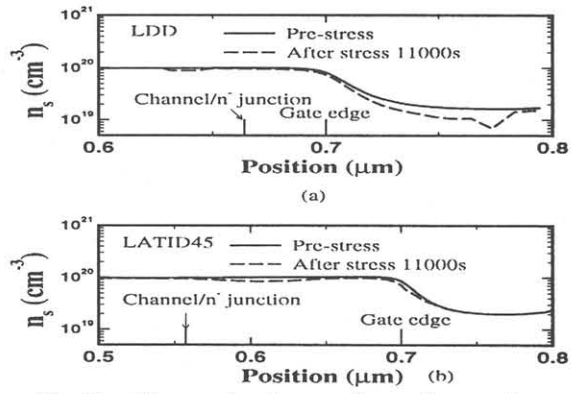


Fig. 7 The reduction of surface electron concentrations after 11000s stress for the devices (a) LDD, (b) 45° LATID.